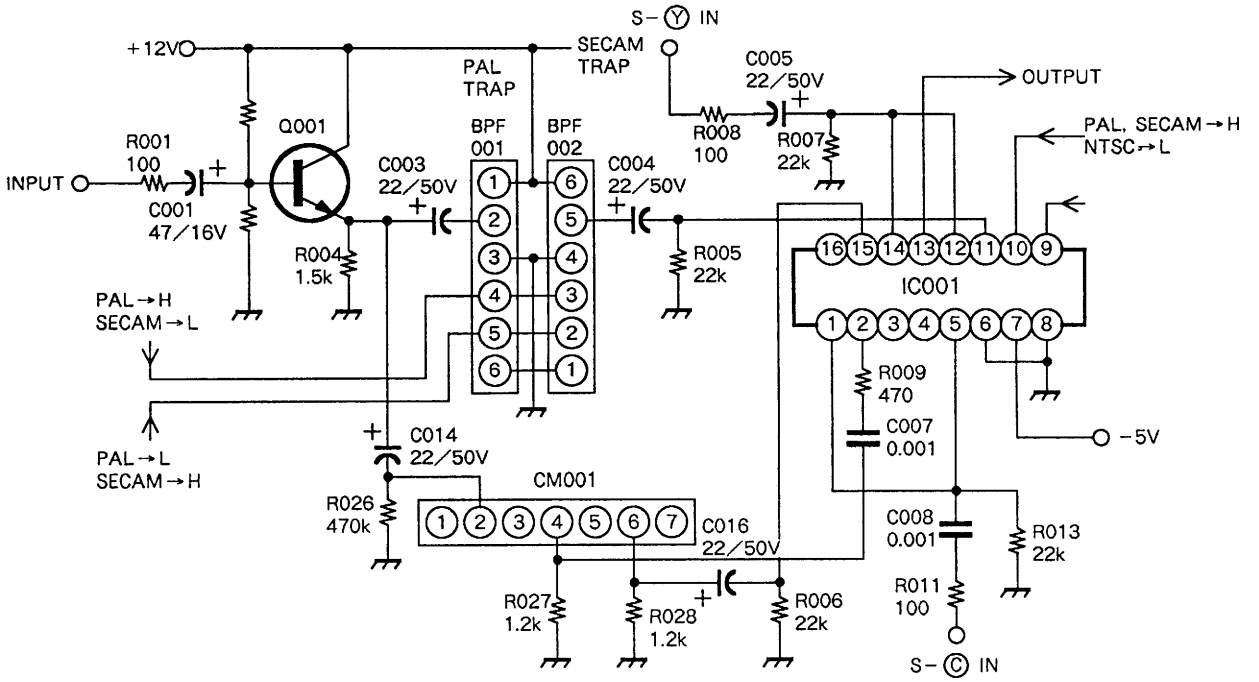
SECTION 3
CIRCUIT DESCRIPTIONS

3-1. Circuit Board BA

Y SIGNALS

1. The TRAP Circuit

The TRAP circuit receives video signals after the signals are fed through Q001. The TRAP circuit is used to extract the chrominance portion of the video signal. However, since this device is equipped to receive 3 types of chrominance frequencies (SUB CARRIERS), namely PAL, SECAM, NTSC 3.58 and NTSC 4.43, it is necessary to switch the TRAP circuit for each type of signal (except for PAL and NTSC 4.43 whose SUB CARRIERS are identical).



<PAL Mode>

Video signals are first input into pin ② of BPF001 wheresignals in the vicinity of 4.43MHz are extracted. The signals are then sent out through pin ⑥ and are input into pin ① of BPF002. BPF0011 and BPF002 are respectively a PAL TRAP and a SECAM TRAP, while pin ④ of BPF001 provides PAL CONT and pin ⑤, SECAM CONT. In all cases, the TRAP is activated when the respective pin signals are High. When operating under the PAL mode, pin ④ will become High and pin ⑤ Low ; the signals pass through BPF002 and appear on pin ⑤ after which they are input into pin ⑪ of IC001. This chip is a switching IC used to switch between PAL, NT 4.43, NT 3.58 and YC signals. Recall that NTSC 4.43 and PAL employ the same method.

<SECAM Mode>

The steps followed are identical to PAL up to the point where the signals are input into pin ① of BPF002. With the SECAM mode, however, pins ④ and ⑤ of BPF001 will both turn High. After signals in the vicinity of 4.43MHz and 4.25 MHz are extracted, the signals are then output from pin ⑤ of BPF002 and input into pin ⑪ of IC001.

<NTSC 3.58 Mode>

Y signals are input into pin ② of CM001 (Comb Filter) while pin ⑥ and pin ④ output Y signals and chrominance signals respectively. Y signals are input into pin ⑮ of IC001 and chrominance signals into pin ② of this IC.

<B/W Signals>

B/W signals are input into pin ③ of BPF001, and are output from pin ⑤ of BPF002. This is a thru output obtained when the control terminals of BPF001 (pins ④ and ⑤) are Low and both traps are disabled. Subsequently, it is input into pin ⑪ of IC001.

2. YC Signals

YC signals are fed to board BB in the form of S-VIDEO -input. Y signals are input into pins ⑫ and ⑭ of IC001 while C signals are input into pins ① and ⑤.

3. IC001 (HD24052BP)

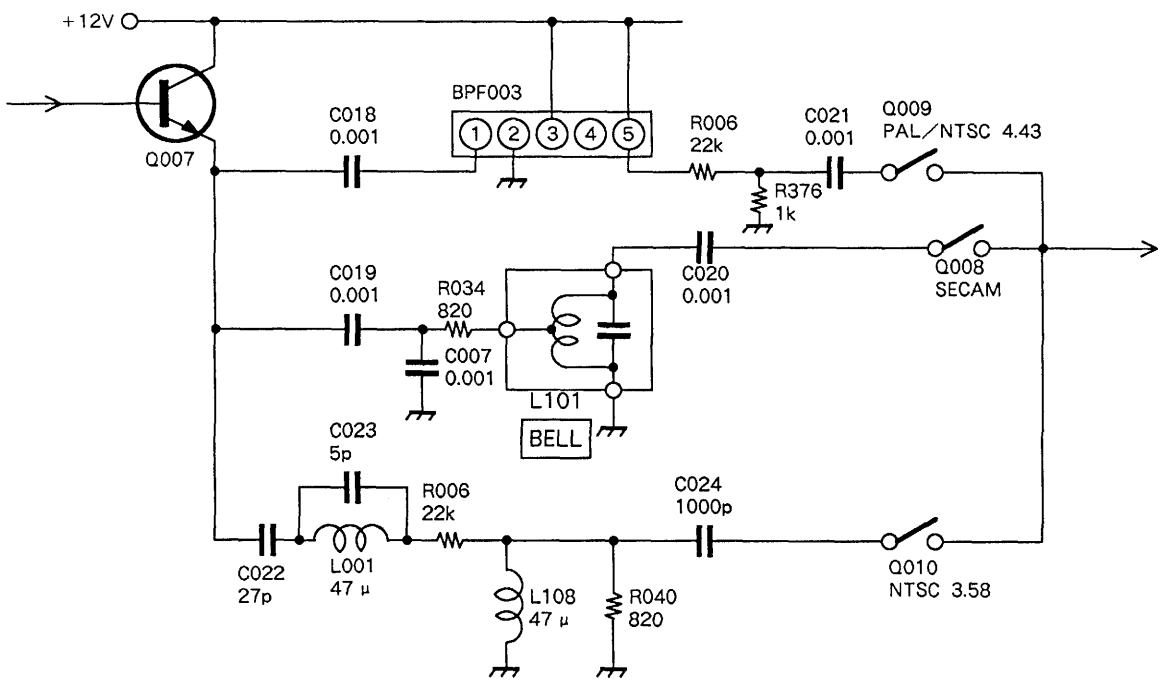
This IC switches between PAL, SECAM, and, NTSC 4.43/NTSC 3.58/YC modes. Outputs appears on pin ⑬ for Y signals and pin ③ for chrominance signals. The signal status of the controller terminals, pins ⑨ and ⑩, are shown in the following diagram. {diagram}

	⑨	⑩
PAL • SECAM • NT4.43 • B/W	H	H
NT3.58	H	L
YC	L	–

4. SHARPNESS IC

Y signals output from pin ⑬ of C001 pass through the Delay Line ; AMP Q003, Q004, and Q005 ; and finally the CLAMP circuit (Q212, 213). The signals are then input into pin ⑬ of IC005. The signals also serve as input signals for board BC (IDTV board) ; these are output from BA-1 31a.

The 2Y signals received from the BC board are switched by IC005 and output from pin ⑭. They are then input into pin ② of IC010 (SHARPNESS IC). The control terminals pins ⑨, ⑩ and ⑪ are High for VIDEO mode and Low for IDTV mode. For IC010, signals was peaked at about 3.6MHz for VIDEO mode and at approximately 6.6MHz for IDTV modes and are output from pin ⑩. Pin ⑧ is the sharpness control terminal ; control voltage is -2.5V to 2.5V. Signals output from pin ⑩ are input into pin ⑦ of R. G .B . MATRIX IC003 (CXA-1216P).



CHROMINANCE SIGNALS

PAL, SECAM, and NTSC 4.43 signals pass through Q001 and after DC cut at C009, are input into pin ④ of IC001. NTSC 3.58 signals go through COMB FILTER CM001 while Chrominance signals are input into pin ② of IC001. After being output from pin ③ of IC001, each signal is passed through a band-pass filter. This circuit is shown below. (circuit diagram)

1. IC002 (TDA4555V8)

Chrominance signals are input into pin ⑮ of the decoder IC002 (TDA4555V8) after they are passed through the respective BPF. PAL and SECAM signals are output from pin ⑫ and fed through the DELAY LINE. The signals are then 1H delayed and input into pin ⑩. After the phase and level are adjusted by L103 and RV101, decoding takes place by adding the signals input from pin ⑮. Subsequently, the R-Y signals are output from pin ①, and the B-Y signals from pin ③. In the case of NTSC signals, the signals are decoded with out passing through the DELAY LINE ; the R-Y signals are output from pin ① while the B-Y signals are output from pin ③. ↗

2. CLAMP CIRCUIT

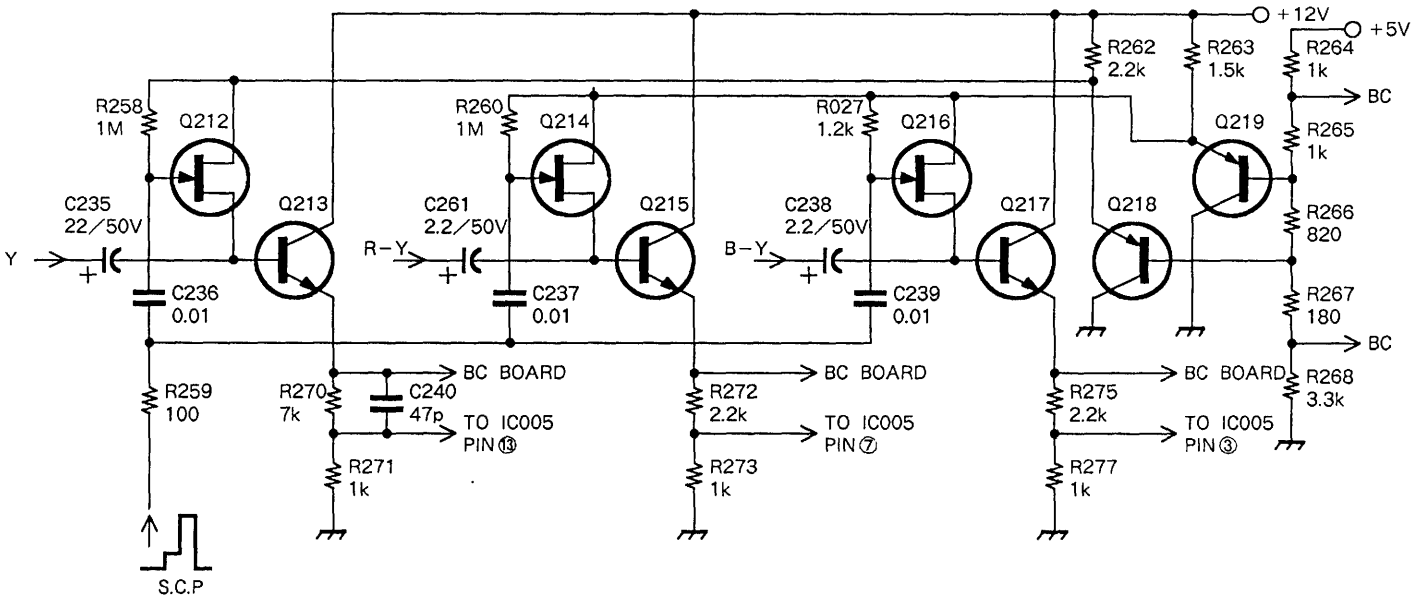
The color-difference signal output from IC002 goes through the CLAMP circuit and enters IC005, an IC used for switching between IDTV. The operation of IC005 is identical to that of the Y signal. Output signals from IC005 are input into an R. G. B. MATRIX IC003 (CXA-1216P).

The ID circuit is comprised of the following 3 of circuits.

a) A phase discriminator. This circuit compares the burst signals for PAL and NTSC modes against its internal reference signals.

b) Frequency discriminating circuit which is used to derive the H/2 signal in SECAM transmissions. It consists of an internal frequency discriminator and an external phase shift detector circuit, connected to pin ㉒ (SECAM ID reference circuit).

c) A logic circuit that provides H/2 signal detection for PAL and SECAM modes, in addition to its original ID function.



3. HUE/COLOR CONTROL

A HUE/COLOR CONTROL voltage ranging from −2.5V to 2.5V is sent to operational amplifire IC012 where the control voltage of CXA1216P is converted to between 2V and 7V.

Because of inconsistencies in IC and resistors, adjustments are made using 3 volumes controls, namely SUB HUE (RV102/VOL for NTSC), HUE ADJ (RV204) and SUB COL (RV205).

4. SUB BRIGHT/SUB PICTURE

Pin ㉗ of IC003 (CXA−1216P) is the CONTROL terminal for PICTURE while pin ㉓ is for BRIGHTNESS. The PICTURE level output is changed by rotating RV203 (SUB PIC) ; turning RV201 (SUB BRT) changes the blackness level.

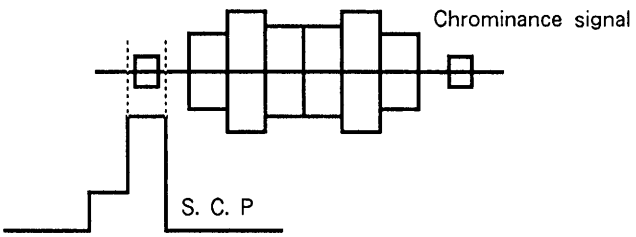
IC004 (TDA2595)

Y signals are first passed through the DELAY LINE and then to AMP Q003/004/005 after which they are fed through the SYNC CHIP CLAMP circuit, comprised of Q352 /351. Finally, the signal is input into pin ⑪ of IC004 (TDA2595). IC004 outputs the sandcastle pulse to pin ⑥ and C. Sync pulse to pin ⑨. The sandcastle pulse is input into pin ㉔ of IC002 (TDA4555−V8) while it also goes into the CLAMP circuit. C. Sync goes into the sync sep circuit, resulting in the output of H. SYNC and V. SYNC pulses. H. SYNC is sent to pin ⑬ of IC006 (TC74HC157AP) via R240 while it is also input into the BC board where it becomes 2H. SYNC and input into pin ⑭ of IC006.

V. SYNC is input into pin ⑩ of IC006 via collector Q207 as well as into the BC board where it is converted to 2V. SYNC. The latter signal is input into pin ⑪ of IC006.

Signals converted by IC006 are output as follows : H. SYNC from pin ⑫, V.SYNC from pin ⑨ and connector BA−1 a−3 HD (1) C−3 VD (1). The C. BLK signals from pin ② of IC004 are merged with the C.BLK signals (BA −1 C−23) input from the DA board and fed into pin ① of IC003

The diagram to the right indicate the phase relationship of pin ⑮ of IC002, the chrominance signal and S. C. P of pin ㉔.



IC009 (CX-7916)

CX-7916 detects between 50Hz and 60Hz by receiving H. SYNC on pin ① and V. SYNC on . ⑤.

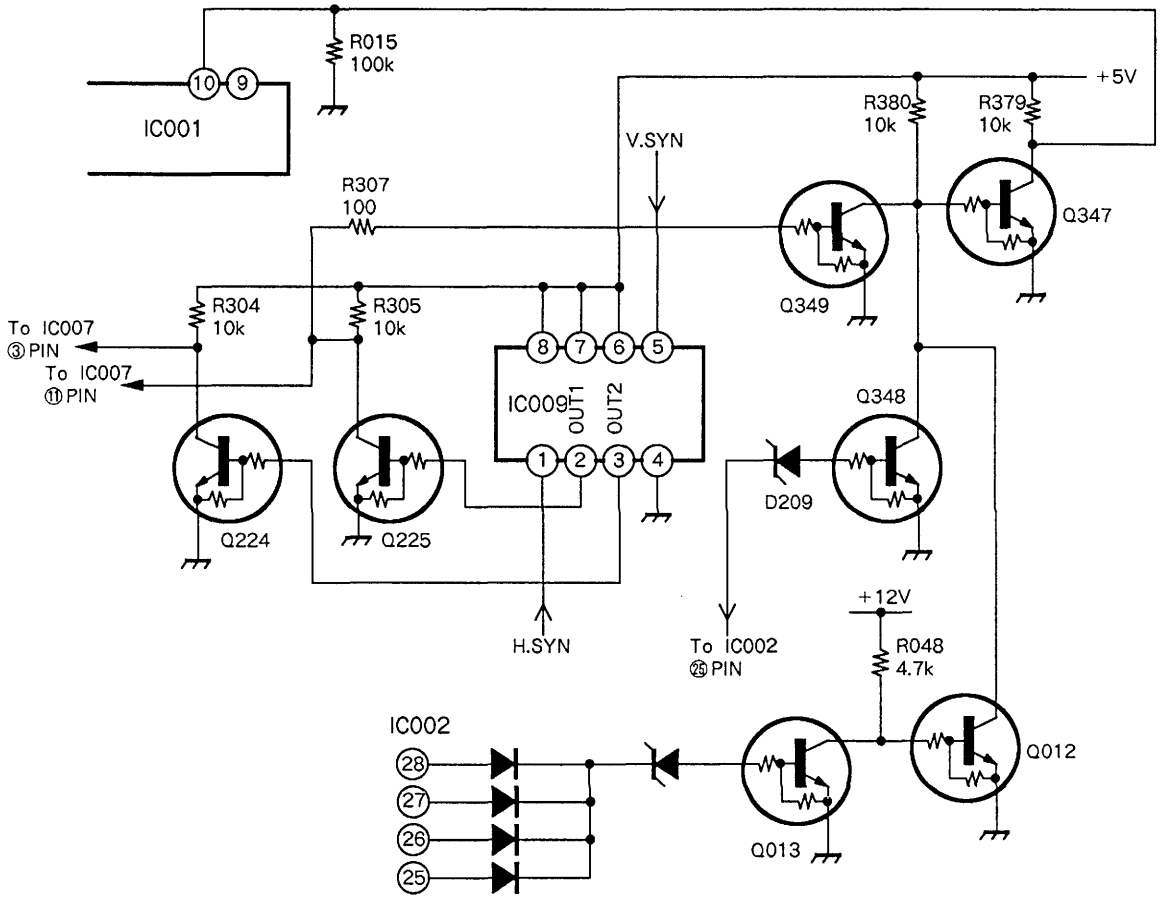
INPUT	②	③
50Hz (PAL、SECAM)	L	H
60Hz (NTSC 3.58 4.43)	H	L

The operation of the peripheral circuitry of IC009 are as follows :

1. NTSC 3.58
Pin ② of IC009 becomes High and Q225 turns ON, making collector Q225 Low while Q349 is turned OFF and the collector becomes High. Further, Q347 becomes ON and the collector Low, causing pin ⑩ of IC001 to become Low.

3. NTSC 4.43
Pin ② of IC009 turns High, providing the same operation asNTSC 3.58. However, since Q348 becomes ON and the collector Low while pin ㉕ of IC002 is High, pin ⑩ of IC001 becomes High.

4. B/W
When color signals are being received, pin ㉕, ㉖, ㉗, or ㉘ of IC002 will be High. In addition, Q013 is turned ON causing the collector to be Low while Q012 is turned OFF causing the collector to be High. These results in the previously described operation. For B/W signals, however, Q013 does not turn ON, and the collector will be High and Q012 turned ON, causing the collector to drop to Low. As-a result, Q347 will be OFF and pin ⑩ of IC001 will be High.

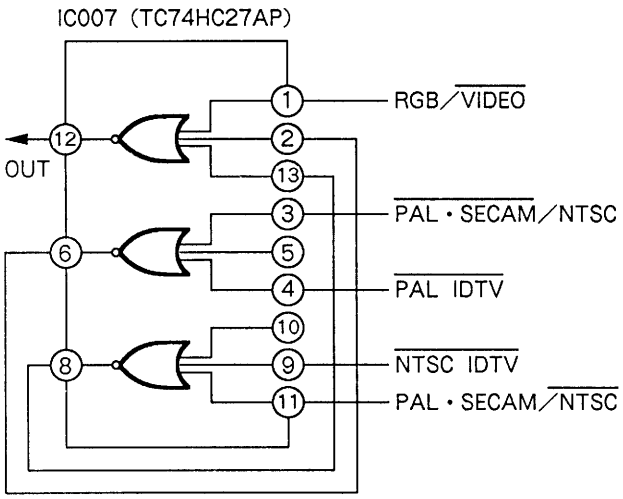


2. PAL/SECAM
Pin ② of IC009 becomes Low while Q225 is turned off and the collector becomes High. Q349 turns ON and the collector becomes Low, causing pin ⑩ of IC001 to turn High when collector Q347 becomes High.

5. IC003 (CXA-1216P)
IC003 (CXA-1216P) is an R. G. B. MATRIX IC. Pin ⑦ inputs Y signals, pin ⑥ inputs B-Y signals and pin ⑤ R-Y inputs while pin ① receives the BLK pulse (refer to section on IC004) and pin ③ receives the B. P. CLAMP pulse. Pins ⑮, ⑰, and ⑲ outputs B, G and R signals respectively.

6. a) DYNAMIC PICTURE SW.
Pin ⑪ of this IC003 is an auto−pedestal which activates the dynamic picture when SW1 is in the open position.

b) IC007 (TC74HC27AP)
This IC is an IDTV (BC board) SW whose pin ⑫ becomes Low in IDTV MODE, High in VIDEO MODE and Low in RGB MODE.
This line controls pins ⑨, ⑩ and ⑪ on IC007 (control terminal for switching signals Y, R−Y, B−Y for VIDEO and 2Y, 2 (R−Y), 2 (B−Y) on the BC board) ; pin ① of IC006 (control terminal for H. SYNC signal for VIDEO and 2H, 2V. SYNC signals on the BC board) ; and finally, pin ④ of IC010 (control terminal for sharpness control).



3-2. Circuit Board BB

RGB INPUT (VIDEO SECTION)

The RGB signals received through Input A or B are each input into pin ⑧ of RL401, 402, 403, after passing through 7A, 9A, 11A of connector BB−1. On the other hand, the RGB signals received through the switcher and CCQ are input into pins ⑬, ⑪, ⑨ of connector BB−2. These signals are then input into pin ⑭ of RL401, 402, 403. Pin ① of RL is controlled according to the mode shown in chart 1 and either of the signals output from pin ⑪ goes into C651, C660, C668.

Chart 1

SLOT SEL (BB-1 23B)	RL401, 402, 403 Pin ①	RL Output Pin ⑦
H	H (CCQ)	Pin ⑭
L	L (INPUT A, B)	Pin ⑧

The red signal is clamped by a clamp circuit comprised of Q666, IC410 so that the pedestal level of the signal fed through Q667, 650 is identical to pin ⑤ of IC410. After clamping, the signal passes through Q670, 674, 678 ; an AMP section comprised by Q682, 683, 684, 685, 686 and is output from 17B of connector BB−1. The circuit of the blue signal is similar and the signal is output from 19B of connector BB−1. As far as the green signal is concerned, the signal passes through a clear blue circuit (refer to page P−14) after which it follows a similar path and is output from 18C.

VIDEO INPUT (VIDEO SECTION)

Signals from this device'S VIDEO IN terminal passes through R539 and the buffer of Q509 and are input into pin ⑫ of IC404. Moreover, as far as the signals received through the S−terminal IN terminal is concerned, Y−signals are input into pin ② of IC404 after passing through Q516, while the C−signals are inputs into pin ⑤ after passing through Q517. On the other hand, the VIDEO, Y/C signals entered through INPUT A, B, each goes through the RGB signal line and inputs into pin ⑧ of RL401, 402, 403. VIDEO, Y/C signals received by the switcher are similarly input into pin ⑭ of RL401, 402, 403. As previously mentioned for RGB input the switch of RL, each output goes into ⑬, ①, ③ of IC404 after passing through Q506, Q507, Q508. At this point, pins ⑨, ⑩, and ⑪ of IC404 is under the mode control shown in chart 2. VIDEO signal, Y−signal, C−signal are output from pins ⑭, ⑮, and ④ after which they are sent out through connector 5C−4B, 5B to the BA board. The RGB signals decoded by the BA board are input to connectors 8C, 9C, 10C on the BB board side where they are respectively fed through Q669, 687, 706 as well as the VIDEO/RGB SW. They are then passed through the emitter follower on Q674, 692, 711 and are output from BB−1 connector 17B, 18C, 19B, following a similar path as that for RGB inputs.

Chart 2

V. IN SEL (BB-1, 23A)	IC404 ⑨, ⑩, ⑪	IC404 Output ⑭, ⑮
H	L (VIDEO IN)	⑫, ②, ⑤
L	H (Others)	⑬, ①, ③

SYNC SECTION

External SYNC

HD, BD received by INPUT A, B are fed into connector 1A, 2A of BB−1 and are input into pins ⑭ and ⑪ of IC405. On the other hand, signals received by the switcher are input into pins ⑦ and ⑥ of BB−2. For this input and in the case of HD, the peak signal is clamped at 0.7V by D501 after being terminated by R501. After this operation, Q501 and Q502 does the switching and a 5Vp−p pulse is output from the collector of Q502. The pulse is then input into pin ⑬ of IC405. VD also goes through a similar circuit, with the pulse being output from the collector of Q504 and input into pin ⑩. The operation of IC405 is controlled according to the modes shown on chart 3; the pulse is output from pins ⑫ and ⑨ and are input into pins ⑬ and ⑩ of IC407.

Chart 3

SLOT SEL (BB-1、23B)	IC405 Pin ①	IC405 Output Pin ⑫, ⑨
H	H	⑬, ⑩
L	L	⑭, ⑪

On the other hand, in the case of VIDEO inputs, sync sep is handled by board BA. Subsequent to this operation the signals go to connector 4A and 5A of BB−1 and are input into pins ⑭ and ⑪ of IC407. IC407 is controlled according to the modes indicated on chart 4 whereby the outputs go from pins ⑫ and ⑨ and connector 26C and 26A of BB−1.

Chart 4

V. IN SEL (BB-1, 23A)	IC407 Pin ①	IC407 Pin ⑫, ⑨, ⑦
H	L	⑭, ⑪, ⑤
L	H	⑬, ⑩, ⑥

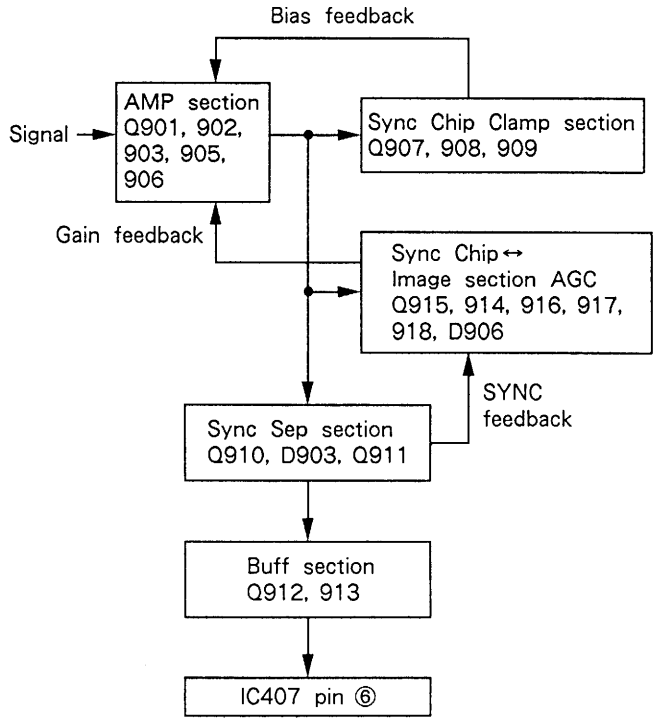
Sync on Green

Green signals from the switcher and from INPUT A and B are, as mentioned earlier, switched by RL402 and input into pin ⑦ of IC401. When the HDVS board is used instead of INPUT A and B, ternary sync pulse is received from connector 16C of BB−1. IC401 is controlled on the basis of the modes shown on Chart 5 and the output comes from pin ④. These output signals pass through C903 and are then sliced by sending them through the AGC circuit, finally sync sep OUT is output from the buffers of Q912 and Q913.

Chart 5

HD SELECT BB-122A	SLOT SELECT	IC401 Pin ④
L	–	Pin ⑦
Open	H	Pin ⑦
Open	L	Pin ②

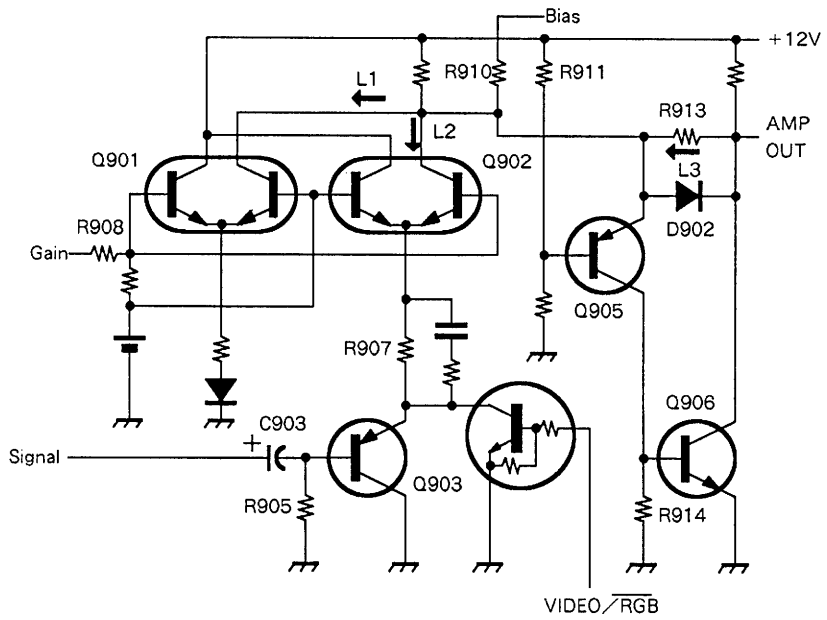
Sync on Green Sync Sep Block Diagram



The sync sep output is input into pin ⑥ of IC407. On the other hand, during VIDEO input, H sync is input into pin ⑤ while pin ⑦ outputs the signals converted by the mode indicated on Chart 4. The converted signals are then input into connector 25C of BB−1.

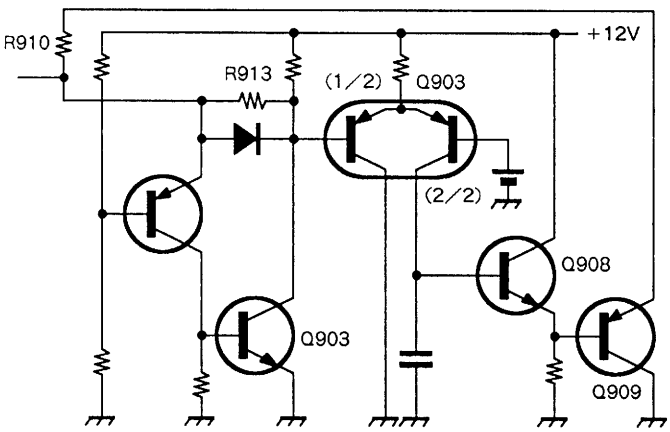
The operation of each section of the sync sep circuit is shown below.

AMP SECTION



Signals are passed through C903 and the signals biased by R905 are converted to an electric current by Q903. This current goes from R907 and flows to emitter Q902. At this point, the signal current, adjusted by the gain control voltage while passing through R908, flows into the collector of Q902. Meanwhile, since the voltage of collector Q902 is fixed at the base electric potential of Q905 $+V_{BE}$, return voltage flows from R913 so that this electric potential remains unchanged. A reverse waveform appears on collector Q906. Therefore, the maximum gain can be expressed as (R913) /R907. Also note that D902 is a limiter for instances when the electric potential of collector Q906 becomes lower than the base electric potential of Q905.

BIAS SECTION



Signal appearing on collector Q903 goes into the base of Q907 (1/2) and is compared against the base voltage of Q907 (2/2) (the voltage determined by R918, 921, 928, 933 and 934). As shown in Fig. 1, for example, if the base electric potential of Q907 (2/2) existed on the waveform's sync section electric potential, Q907 (2/2) of only the sync section is turned ON and the Q908 base electric potential increases, resulting in an increase of the base of Q909. As a result, the DC current that flows from R910 to Q909 decreases and the electric potential of collector Q903 decreases as well. Finally, R910 releases electric current so that the highest point of the base electric potential of Q907 (1/2) and the base electric potential of Q907 (2/2) are the same.

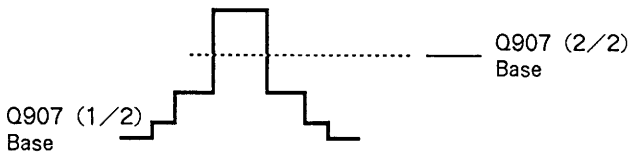
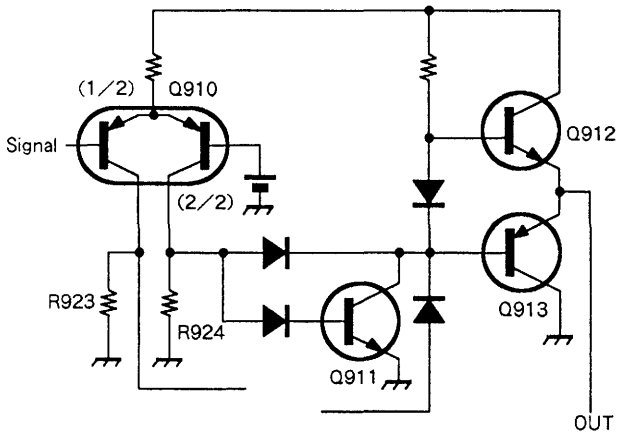


Fig. 1

SYNC SEP SECTION



The signal generated by the AMP section (described earlier) is input into Q910 (1/2) and the DC voltage as determined by R918, 921, 928, 933 and 934 is input into Q910 (2/2). The relationship in voltage between the two is demonstrated in Fig. 2 where it can be seen that Q910 (2/2) is turned ON only starting from the Sync section. Other sections become Low. This pulse is switched by Q911 and is extracted as 5V negative composite sync.

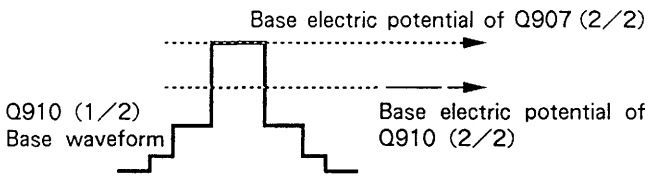
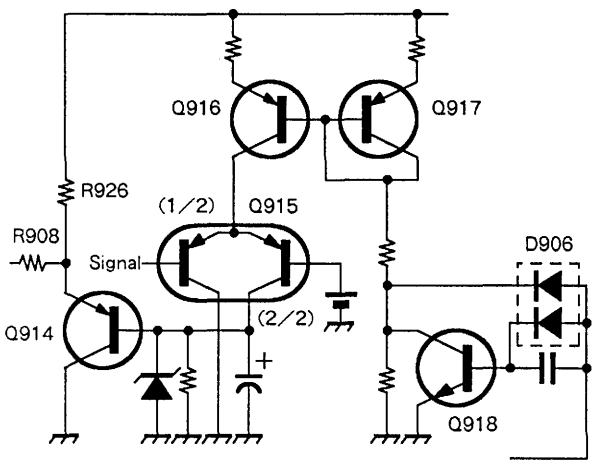


Fig. 2

GAIN CONTROL SECTION



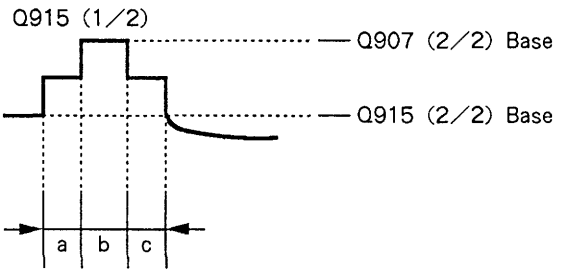
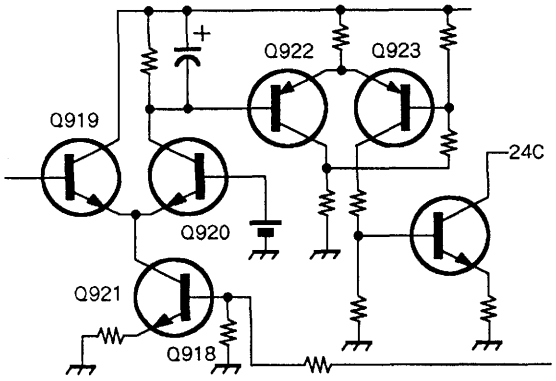


Fig. 3

The output from AMP is input into the base of Q915 (1/2) while the electric potential as determined by R918, R921, 929, 933 and 933 is fed into R915 (2/2). This means that the one with the lower base voltage is turned ON. On the other hand, sync sep out (negative polarity) that appears on collector terminal Q910 (1/2) is input into Q918. This is turned ON only during the time the sync section is operating. Subsequently, current flows into Q917, and the same current flows into Q916. As a result, supposing that a waveform similar to that shown in Fig. 3 is input, Q915 (2/2) is turned ON during a and c, the electric potential of collector Q915 (2/2) as well as that if emitter Q914 increases. When this occurs, as described earlier in the AMP section, the electric potential of the gain control terminal increases, making the AMP's gain increase. It is through this type of operation that the difference in electric potential between the pedestal section and the sync CHIP section becomes the base electric potential variance between Q907 (2/2) and Q915 (2/2).

Ternary Sync Discriminating Circuit



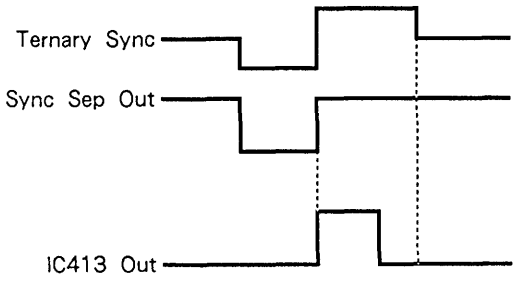


Fig. 4

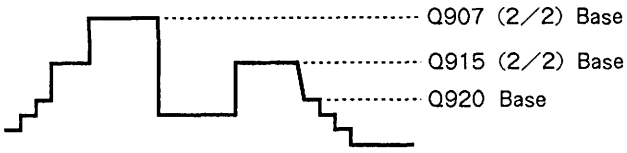


Fig. 5

AGC and clamped signals produced by the previously mentioned sync sep circuit are input into the base of Q910 while the DC voltage shown in Fig. 5 is added to Q920. Furthermore, Q921 is connected to the emitters of Q919, and Q920, and the pulse shown in Fig. 4 is entered into their bases, making the system ON only when the voltage is higher than the pedestal's ternary sync voltage.

As a result, whenever ternary sync is input, Q920 turns ON only when the voltage is higher than the pedestal's and the electric potential of collector Q920 falls. This is recharged by C911 and transmitted to the base of Q922.

Q922 and Q923 are schmitt trigger circuits whereby when the base electric potential of Q922 falls, Q923 becomes OFF, lowering the collector electric potential and turning Q924 OFF.

AUDIO SECTION

The signals connected to the switcher (R, L, MIX) are input into pin ② of IC408, 409 via pin ① of connector BB−2. In addition, the R and L signals input into INPUT A and B are fed into 13A and 14A of connector BB−1 and enters pin ⑫ of IC408. IC408 and 409 are controlled by the mode shown in diagram 6 and output through pin ⑭. The R, L signal is then input into pins ⑥, ④ of IC412, increased or reduced according to the changes in the VOL control terminal voltage of pins ② and ⑧, and output from pins ⑦, ③ as well as from 3C, 3B of connector BB−1.

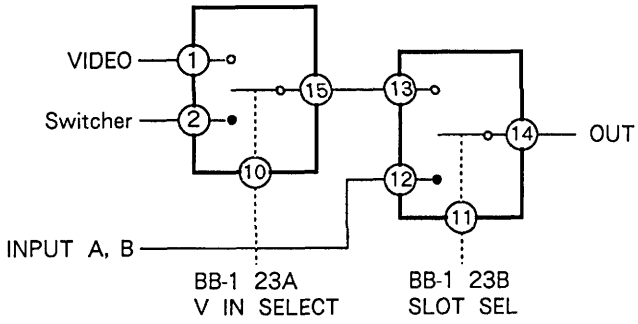


Fig. 6

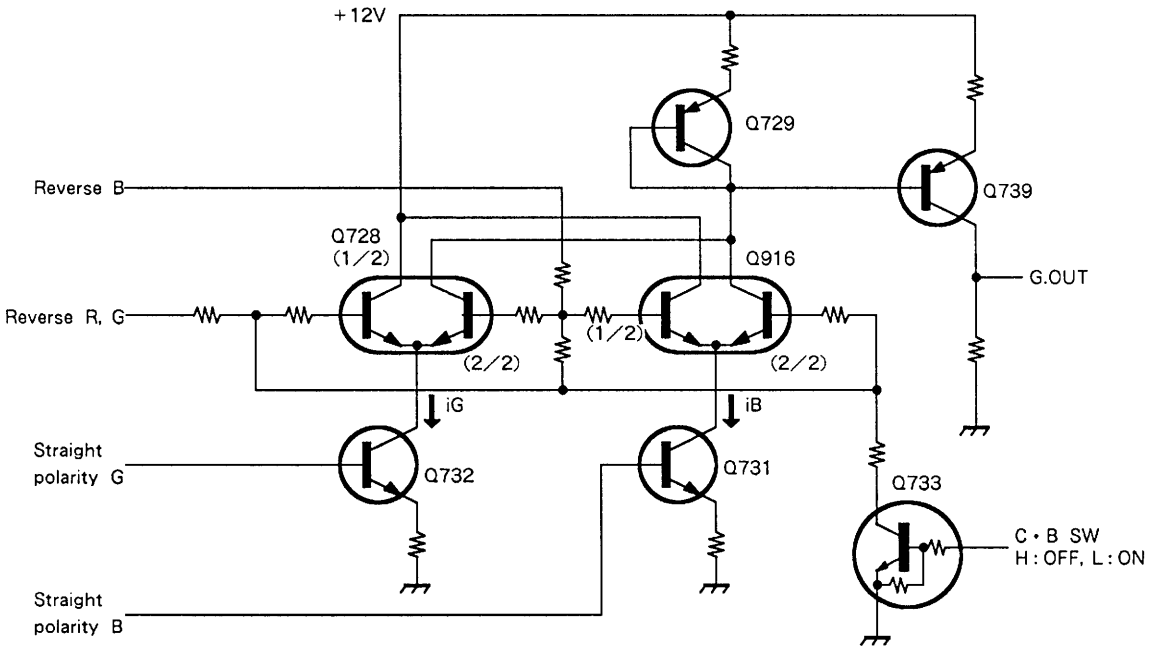
SIRCS SIGNAL

Signal received by the optical receptor of this unit goes into 1C of connector BB−1, the signal from the attached remote control unit to 1B of connector BB−1, and the signal from the switcher are input into pin ② of BB−2 respectively. Signal received at the optical receptor unit takes the following pass : Q450, 451 to SW included in the SIRCS IN terminal, to D450, to Q454 and finally to 23C of connector BB−1. In addition, it is also sent to SIRCS OUT via Q456. At this point, the included SW turns OFF when a terminal is inserted into SIRCS IN, and ON when removed. Therefore, when the terminal is plug the WIRELESS input on the main unit is disabled. Instead, the plug WIRED input signal is sent to D450. On the other hand, the signal from the main unit's remote controller goes into D450 after which it follows the same path. Furthermore, signal from switcher is sent to Q453 and after that is the same.

CLEAR BLUE CIRCUIT

The clamped R (red) signal appears in reverse waveform at collector Q667. This is sent to Q668 and the G (green) signal is similarly sent to Q727. As result, the signal that appears on emitter Q668 and 727 is a signal with low base electric potential (signal with a higher image level). This is sent to the base of Q728 (1/2) and 730 (2/2) via Q728. On the other hand, B (blue) signal appears in reverse waveform on collector Q737 and is sent to Q736 after which it is sent to the bases of Q728 (2/2) and 730 (1/2) via R740 and 743. At this point, for R and G signals the DC level is determined by the power supply from Q734 when it is reversed. While the DC level for B signal is determined by the power supply from Q735. Furthermore, the emitter of Q728 is connected to collector Q732 and the G signal current flows as result of the G signal input into the base. Likewise, the emitter of Q730 is connected to the collector of Q731 and the B signal current flows as result of the B signal input into the base. First of all, when the C. B SW is in the OFF position Q733 turns ON and the base electric potential of Q728 (1/2) and 730 (2/2) becomes low. ↗

As result, Q728 (1/2) and Q730 (2/2) turns OFF ; Q728 (2/2) and Q730 (1/2) turn ON ; a reverse waveform of G signal appears on collector Q729 after which it is reversed by Q739 and input into Q688. When C.B SW is ON, the base electric potential of Q728 (1/2) and Q730 (2/2) are compared against the base electric potential of Q728 (2/2) and Q730 (1/2). The transistor with higher base electric potential is turned ON. As result, if the signal level of B signal and R, G signal is compared and if the B signal level is higher Q730 (2/2) and Q728 (1/2) are turned ON and a MIX signal of B signal and G signal is output to collector Q729. In case, the B signal level is lower than the signal level of R,G, Q730 (1/2) and Q728 (2/2) turn ON and only the G signal is output to collector Q729. As shown above, CB operation produces G signal to B signal and turns blue to cyan.



TEST SIGNAL GENERATOR

When the test signal mode is selected, 27C of connector BB−1 becomes low and collector Q656 becomes high. It then passes through D652, 653 and turns Q671, 672 ON when R, Q689, 690 when G and Q708, 709 when B and turns OFF the RGB and VIDEO signals. On the other hand, test signal are input into each RGB signal via Q675, Q693 and Q712.

Signal (hatched, dotted, and other test signal) Generator Section.

ECL signals are input into 28A, 28B of connector BB−1 and the respective signals are input into Q660, 661. The lighting portion of the test signal turns the Q660 side High and Q661 Low. As result, Q660 and Q665 becomes ON and electric current flows into collector Q654 through a current mirror circuit. Then a voltage is generated by R659, R663, and R655 (described later) and is input into Q652. This signal is added to each of the RGB circuits.

C. BRT Signal (signal that increases or lowers brightness of the image during ZONE MODE) Generator Section.

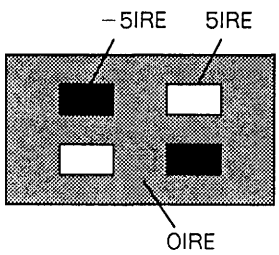
ECL signals are input into 28C, 29C of connector BB−1 and are respectively input into Q663 and Q665. For normal test signals, the base of Q663 becomes Low and since Q665 is already High, Q663 turns ON and current flows through Q664 and Q662. On the other hand, under the ZONE MODE, excluding the area which is to emphasized, the base of Q663 turns High and Q665 becomes Low, making Q663 and Q662 both OFF. As a result, the current that flows through Q660 as well as Q654 decreases, causing the base electric potential of Q652 to fall and the brightness to decrease.

BOARDER Signal (the shadowed portion of the character signal) Generator.

ECL signals are input into 29A, 29B of connector BB−1 and the respective signals are input into the base of Q658, 659. When the mode changes to character signal output mode, the character signal plus the shadow portions turn the base of Q658 High, the base of Q659 Low and Q658 becomes ON. Consequently, the base electric potential of Q657 becomes negative (−) and these are transmitted to the bases of Q676, 794, 713 and Q677, 695, 714 turn ON. For this reason, the RGB signals are cut−off by this section and shadow is formed.

PLUGE SIGNAL GENERATOR

Pluge signal is a signal like that shown on the diagram on the left. Signal is input from 27A, 27B of connector BB−1 and respectively input into the bases of Q650, 651. For regular TEST signals, 27A is set to High and 27B is set to Low and the transistor on the opposite side of Q650 signal input side turns ON. Electric current then close to R655 and is transmitted to the base of Q652. For this reason, regular TEST signals will have the MIX signal from Q650 and Q654 added to the base of Q652. In the case of pluge mode for the −5IRE section on the diagram, 27A, 27B both turns Low and since no current flows to R655 the electric potential of Q652 falls. For the 5IRE section, 27A, 27B become High and current flows to R655 from both Q655 and 651 causing the electric potential of Q652 to fall. As result, Pluge signal is generated.



CHARACTER SIGNAL GENERATOR

Each of the RGB character signal are input as ECL signals into 30A, 30B, 31A, 31B, 30C, 31C of connector BB−1. Since the circuit is the same for R, G, and B, the circuit for R only will be explained. Signals input from 30A, 30B are respectively input into the bases Q680, 681. Under normal circumstances, 30A is Low and 30B is High and Q681 is turned ON. Therefore, the base electric potential of Q679 is split by parallel resistance between R703, 961, and R704, 711 and is lower than the electric potential of Q678, causing the input signal to pass through Q678 unchanged and input into Q682. On the other hand, in character mode, the character portion only will have 30A High and 30B Low. Q681 is turned OFF and the base electric potential of Q679 increases. At this point, Q679 turns ON resulting in the input signal and the character signal to be output alternately and input into Q682.

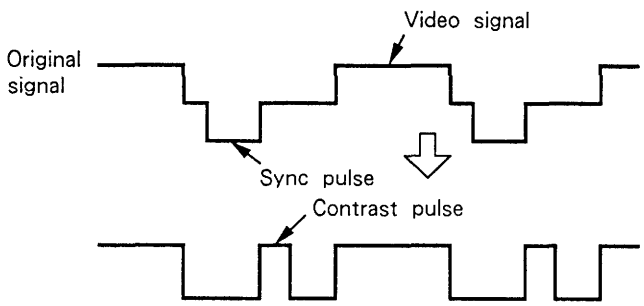
CA (RG) and CA (B) Boards

• STRUCTURE

The CA (RG) board consists of signal processors for RED and GREEN CH. (BKG, DRV, Contrast, and Brightness controls plus cut off SW, blanking system, and pedestal clamp), video output amplifier, final−stage clamp circuit, automatic background circuit, peak ABL, and single−tube ABL circuit. Note that a gamma correction circuit accompanies the RED CH. The CA (B) board includes these functions for the BLUE CH.: signal processing (same features as for CA (RG) board), gamma correction circuit, video output amplifier, final−stage clamp circuit, automatic background circuit ABL circuit, and G1 blanking circuit.

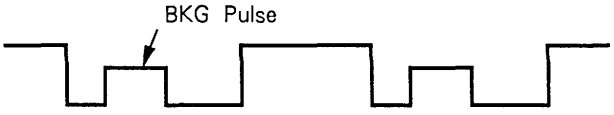
• SIGNAL PROCESSING

BKG, DRV, Contrast, and Brightness control ; cutoff SW ; blanking and pedestal clamp signal processing are managed by IC104 (RED CH), IC204 (GREEN CH), and IC304 (BLUE CH). Signals input into pin ㉖ through AC merging are first clamped by a back port and a reference pulse (contrast pulse) for gain control (see diagram below) are inserted.

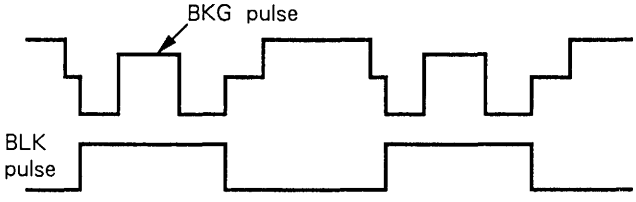


The pulses are then sent through a gain control amplifier (DC control) after which a feedback is applied so that the control pulse becomes as large as a certain reference value. This circuitry enables contrast to be controlled by simultaneously inserting various levels of control pulses while DRV can be controlled by changing the reference value against which the contrast pulse is compared. This circuit design brings about excellent inter-channel tracking performance.

When these processes are completed, instead of the contrast pulse, reference pulses for Brightness and Background control (BKG Pulse) are inserted. Brightness and Background control is carried out by changing the level of this BKG pulse.



As shown in the diagram below, with the exception of the BKG pulse section, blanking is applied by the blanking pulse input from pin ⑤ and the pulse is output from pin ③.



• VIDEO OUTPUT AMPLIFIER

This amplifier makes use of hybrid IC VPH05 (IC101, 201, 301) and is comprised of a cascode amplifier and a complimentary buffer. Note that a peaking terminal is provided in pin ③.

• FINAL-STAGE CLAMP CIRCUIT

This circuit uses a hybrid IC SNY-8C02 (IC103, 203, 303). As the BKG pulse sector is clamped here, the pedestal level can be adjusted by changing the size of the BKG pulse.

• AUTOMATIC BACKGROUND CIRCUIT

(Only the RED CH is explained here, but the explanation is applicable to other CH as well.)

The Ik that is detected by a cathode electric current detecting circuit (comprised of Q104, 105, 106, 107, 112) is converted to voltage and is sent through the voltage follower of IC102 (2/2). The voltage is then S/H'd by Q111 and C119 and the clamp voltage is modified by the previously-mentioned final-stage clamp circuit so that the voltage becomes the same as the reference value.

• SINGLE TUBE ABL CIRCUIT

The electric current detected by cathode electric current detecting circuits Q103 (RED), Q203 (GREEN), and Q303 (BLUE) are converted to voltages and respectively integrated. Q16, 17 and 18 determine which RGB voltage is the largest and this voltage is passed through the reverse phase amp IC8 (2/2). If the voltage is greater than the standard value, Q15 acts to lower the contrast.

• PEAK ABL CIRCUIT

Each electric current that is derived from the above RGB cathode electric current detecting circuits is added by IC8 (1/2) and the contrast is lowered by Q14 if greater than the standard value.

• Σ ABL CIRCUIT

The ABL voltage detected by the secondary side of the flyback transformer goes into the base of Q30 and is compared against the base voltage of Q31. When the flyback current becomes greater than the standard value, the contrast is lowered.

• G1 BLANKING CIRCUIT

The TTL level BLK pulse is amplified to approximately 112Vp-p by circuits Q32 to Q40. They are then supplied to G1 of each of the R.G.B. channels.

3-3. Circuit Board DA

The functions of board DA can be divided into the following :

1. AFC Circuit System
2. Waveform Regeneration
3. Others

1. AFC CIRCUIT SYSTEM

(1) H. SHIFT···AFC achieves synchronization by comparing H. SYNC and HD (Horizontal deflection). When pulse hd is created from HD by shifting a certain phase (r), and if the AFC is then taken with H. SYNC and hd, the AFC of HD will be shifted by −r. Therefore, changing r results in a H. SHIFT.

In practice, the horizontal deflection HD is feed back to connector 7−b after which it passes through buff Q1 and enters IC8, the H. SHIFT circuit. The noise content is removed by SW of IC8 and a pulse is produced by IC9 (1/2) using its leading edge as a trigger. Since the integrated value of output ⑦ of IC9 and Vcc/2 is compared by IC10 (1/2) and feed back, the second diagram of Fig. 1 becomes a short waveform with a 50% duty factor. This output is once again input into IC9 (2/2) and sent through a similar feed back system. If the phase is controlled using the H. SHIFT voltage (−2.5V to +2.5V) from connector 27−b rather than the comparing voltage Vcc/2, a movement of ±22% is observed as shown in the third diagram in Fig. 1. By entering this into IC13 and by creating a rectangular waveform with a 50% duty factor, a pseudo HD pulse for AFC use is realized.

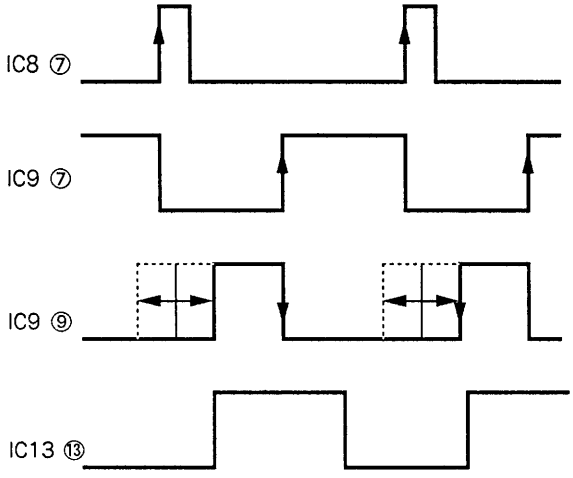


Fig. 1

(2) V. SHIFT···V. SHIFT uses the same method as V. SHIFT to shift the phase of incoming V. SYNC. The circuit is almost the same as that of H. SHIFT. The V. SYNC of connector 9−a is delayed by about 1V with IC11, 12 and the phase shift is accomplished with the V.SHIFT control voltage of connector 27−c.

(3) AFC CIRCUIT···IC14 is a hybrid IC that includes a jungle IC and is responsible for AFC and V. HOLD. In terms of its operation, when H. SYNC is fed into pin ⑧ it does a F−V conversion and outputs a H. OSC waveform from pin ⑨ which corresponds to the frequency's fo. RV1 is used to adjust fo.

For VIDEO operation, pin ① of IC8 becomes "Low", Q27 goes off, and the voltage that is decided by resister division of RV3, R163, 164 is input into pin ⑤. This becomes the fo voltage for VIDEO use.

(4) V. HOLD CIRCUIT···The V. SYNC OUT described in "(2) V. SHIFT CIRCUIT" is fed from Q14 to pin ⑪ of IC14. A F−V conversion is done inside IC14 based on this pulse and VD of fo corresponding to the input frequency is output from pin ⑫ of IC14.

2. REGISTRATION WAVEFORM GENERATOR

(1) REGISTRATION IC SECTION···When VD is input into pin ⑤ of IC201 and HD is input into pin ㉔, registration waveform is created using the leading edge of the input signal as trigger (FIG. 2−1, 2−2). The peak of V. SAW, H.SAW is determined by the voltage of pin ㉗ and ㉕ respectively. Since a parabola wave is SAW × SAW, when the SAW amplitude becomes 1/2 it becomes 1/4. Other waveforms will become 1/4, 1/8 and so forth depending on how many times a multiplication is performed. Pin ③ and pin ④ outputs a rectangular waveform of 1/2H, 1/2V respectively. ↗

(2) V. SIN WAVEFORM···When a full wave rectification is performed with IC208 using the waveform of pin ⑩ of IC201, the waveform of pin ① of IC208 will be like that shown in Fig. 3−a. The parabola wave of pin ⑪ of IC201 is DC−shifted to make the output of pin ① of IC209 as shown in Fig. 3−b. Q205 to 212 comprise a multiplier and when Fig. 3−a and 3−b are entered into this multiplier, a waveform similar to the one shown in Fig. 3−c is produced. This will be divided by IC210 to make the first half of V−scan into V. SIN 1 and the latter half into V. SIN 2.

(3) H. SIN WAVEFORM···As with V. SIN waveform H. SAW will be full−wave rectified using IC217 while H. PARA will be DC−shifted with IC215. Each of these are multiply by Q213 to 220 to create waveforms similar to V. SIN.

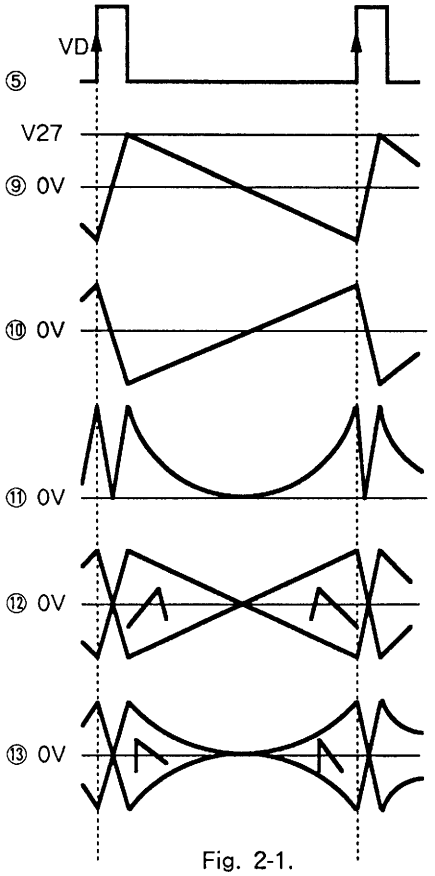


Fig. 2-1.

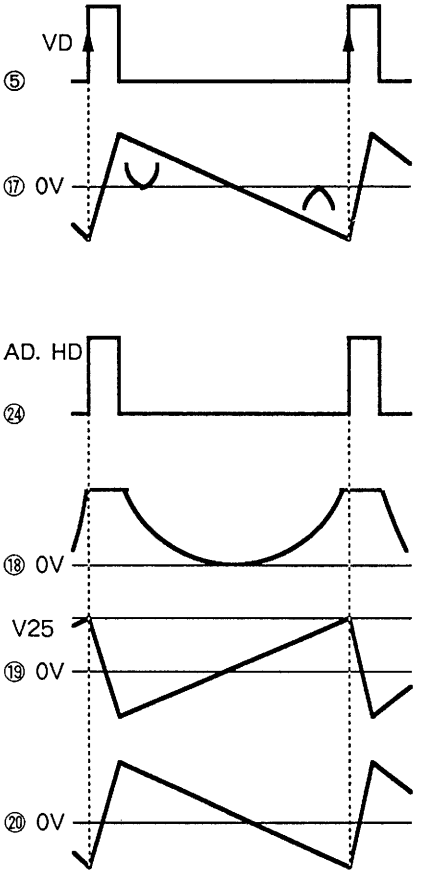


Fig. 2-2.

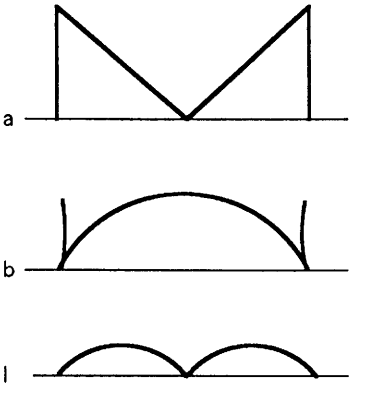


Fig. 3.

3. OTHERS

(1) AD. HD ··· Registration correction is affected by eddycurrent. To rectify this problem regeneration waveforms are created by advancing the waveform by 1 to 2 μs. The horizontal deflection of HD is input into pin ④ of IC3. A constant that will become approximately 3 to 4 μs will be used and integrated (IC3 ⑥). Next the horizontal deflection of HD is input into pin ⑪ of IC3 and a pulse created using the leading edge as trigger. This Q output will be integrated and the result of previous integration will be compared against IC4. Since a feedback is applied, the pulse width of pin ⑥ and ⑨ of IC3 will be the same. As a result, the pulse width of pin ⑨ of IC3 will become 3 to 4 μs. Because the original HD (pin ⑪ of IC3) is about 2 μs, the net effect on the pulse of pin ⑨ of IC3 will be an advancement of 1 to 2 μs. This will be input into IC201 to create a horizontal regeneration correction waveform.

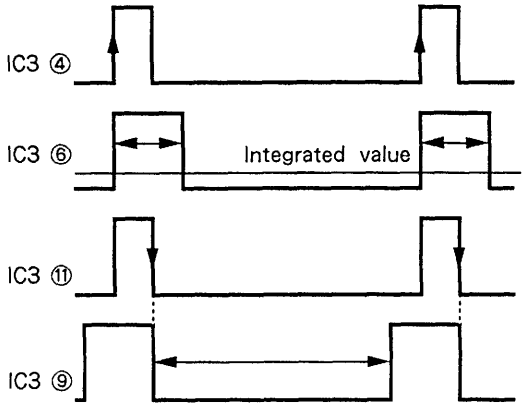


Fig. 4

(2) BLK PULSE

1) V. BLK···The position of BLK has been fixed so that even if the size is altered, the on-screen position of BLK will not change. By performing slice and comparing operations on a certain level of V. SAW, a pulse such as BLK 1 that is shown in Fig. 5 is created (IC220). If the bias of BLK (T) in Fig. 5 is changed, the width of BLK 1 alters. V. BLK is structured by adding a retrace line, as well as VD and V. Pulse so that BLK is effected during a H. STOP.

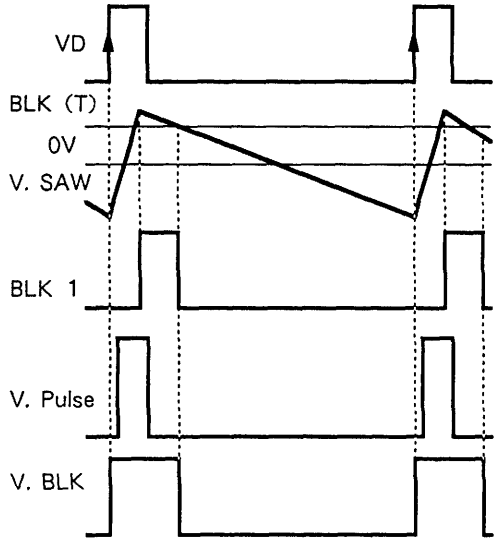


Fig. 5

2) H. BLK···Although similar to V. BLK in principle, since H. SAW is created with AD. HD, if the pulse created by slicing H. SAW with H. BLK (R) and if HD is added to create H. BLK, the phase of the two BLK pulses will not align as shown in Fig. 6, H. BLK 1. For this reason, H. BLK will be created by padding HD.
A pulse is created by shifting the voltage level of connector 25−c and shifting H. SAW (Fig. 7 H. BLK 2). Voltage a will be defined to be the voltage resulting from integration. BLK (R) is created as follows. First add HD to pin ⑪ of IC5 and create a pulse using the leading edge as a trigger. Then take the integrated value of output $\overline{Q}$ (pin ⑨ of IC5), compare it against a in the foregoing, and apply a feedback until the same integration value is obtain. BLK (L) is created in the same manner.

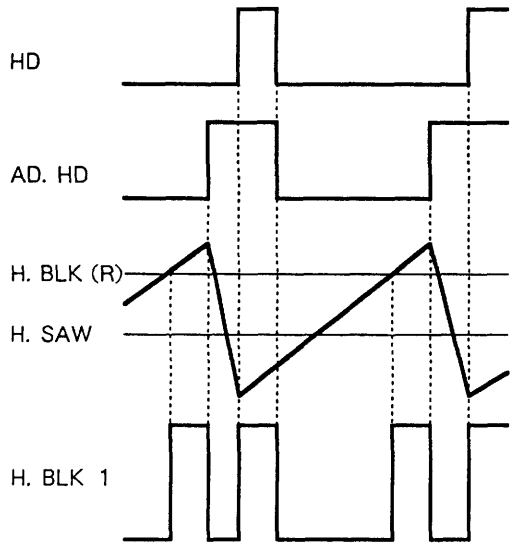


Fig. 6

3) C. BLK···Feed BLK pulses V. BLK (1) and H. BLK (2) through the decoder circuit. C. BLK will be output from pin ⑮ (OUT). Pin ⑮ is an OR output which becomes Low only when pins ①, ②, ③, and ⑥ are also Low.

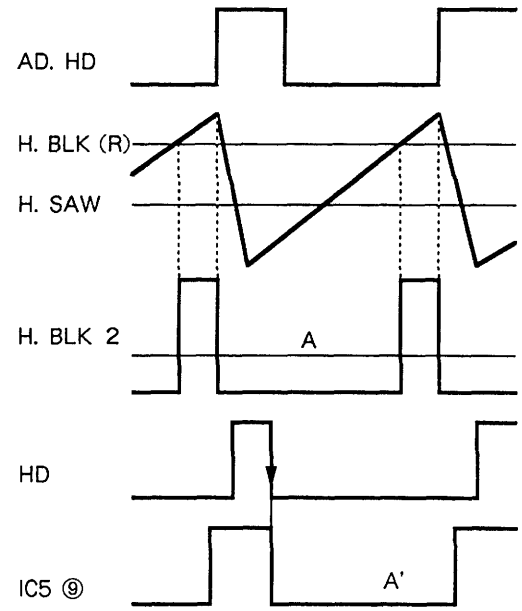


Fig. 7

(3) SIZE ABL CIRCUIT···Since ABL circuit is a total high −voltage limiter, when its size is halved, the current density per unit area is doubled. This can become the cause for partial burning of the tube surface and cracking of the CRT due to heat concentration. This set has a particularly wide size range, the current density can become several times larger. For this reason, a SIZE ABL circuit, which keeps the current density per unit area fixed, was added. Control voltage H. SIZE and V. SIZE are multiplied and the result added to the ABL detection point, as shown in Fig. 8. As a result, the detecting voltage is changed. The ABL is therefore being changed through the use of SIZE.

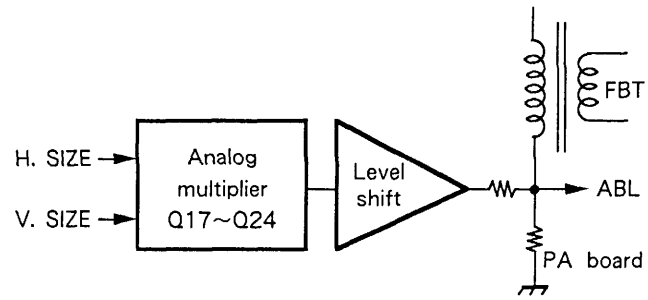


Fig. 8

3-4. Circuit Board DB

This board incorporates functions of conventional regenerator matrix VR as well as those of various other control VRs. The features of D/A converter MB86023 are as follows :

Pins ① to ⑧	...	DATA input (standard input)
Pins ⑨ and ⑩	...	control terminal that selects 1 of 4 possible outputs
Pin ⑪	...	reads DATA upon receipt of a pulse
Pin ⑫	...	activated when low
Pin ⑬	...	digital GND
Pin ⑭	...	analog GND
Pin ⑮	...	−5V
Pins ⑯ to ⑲	...	output
Pin ⑳	...	input for reference voltage
Pin ㉒	...	+5V

The voltage produced in reference to input voltages V1 is 7−V1 for DATA 00, 0 for DATA 80, and V1 for DATA FF. IC501 to 504 are buffers while IC505 to 510 are address decoders. The output and the name associated with each signal are shown below :

IC511 ⑲ H. SIZE
⑱ H. CENT (G) 1
⑰ H. CENT (R) 1
⑯ H. CENT (B) 1

IC512 ⑲ H. SHIFT
⑱ H. CENT (G) 2
⑰ H. CENT (R) 2
⑯ H. CENT (B) 2

IC513 ⑲ H. KEYS
⑱ H. SKEW (G)
⑰ H. SKEW (R)
⑯ H. SKEW (B)

IC514 ⑲ H. PIN
⑱ H. BOW (G)
⑰ H. BOW (R)
⑯ H. BOW (B)

IC515 ⑲ ————
⑱ H. SIZE (G)
⑰ H. SIZE (R)
⑯ H. SIZE (B)

IC516 ⑲ H. LIN BIAS
⑱ H. LIN (G)
⑰ H. LIN (R)
⑯ H. LIN (B)

IC517 ⑲ V. KEYS BIAS (B)
⑱ ————
⑰ H. KEYS (R)
⑯ H. KEYS (B)

IC518 ⑲ ————
⑱ ————
⑰ H. PIN (R)
⑯ H. PIN (B)

IC519 ⑲ V. SIZE
⑱ V. CENT (G) 1
⑰ V. CENT (R) 1
⑯ V. CENT (B) 1

IC520 ⑲ V. SHIFT
⑱ V. CENT (G) 2
⑰ V. CENT (R) 2
⑯ V. CENT (B) 2

IC521 ⑲ V. SIZE BIAS
⑱ V. SIZE (G)
⑰ V. SIZE (R)
⑯ V. SIZE (B)

IC522 ⑲ V. LIN BIAS
⑱ V. LIN (G)
⑰ V. LIN (R)
⑯ V. LIN (B)

IC523 ⑲ ————
⑱ V. SKEW (G)
⑰ V. SKEW (R)
⑯ V. SKEW (B)

IC524 ⑲ ————
⑱ V. BOW (G)
⑰ V. BOW (R)
⑯ V. BOW (B)

IC525 ⑲ V. KEYS BIAS (R)
⑱ V. KEYS (G)
⑰ V. KEYS (R)
⑯ V. KEYS (B)

IC526 ⑲ ————
⑱ V. PIN (G)
⑰ V. PIN (R)
⑯ V. PIN (B)

IC527 ⑲ ————
⑱ H. ZONE 2 (G)
⑰ H. ZONE 2 (R)
⑯ H. ZONE 2 (B)

IC528 ⑲ ————
⑱ H. ZONE 3 (G)
⑰ H. ZONE 3 (R)
⑯ H. ZONE 3 (B)

IC529 ⑲ H. ZONE 4 BIAS
⑱ H. ZONE 4 (G)
⑰ H. ZONE 4 (R)
⑯ H. ZONE 4 (B)

IC530 ⑲ H. ZONE 5 BIAS
⑱ H. ZONE 5 (G)
⑰ H. ZONE 5 (R)
⑯ H. ZONE 5 (B)

IC531 ⑲ ————
⑱ H. ZONE 6 (G)
⑰ H. ZONE 6 (R)
⑯ H. ZONE 6 (B)

IC532 ⑱ H. ZONE 7 (G)
⑰ H. ZONE 7 (R)
⑯ H. ZONE 7 (B)

IC533 ⑱ H. ZONE 8 (G)
⑰ H. ZONE 8 (R)
⑯ H. ZONE 8 (B)

IC534 ⑱ H. ZONE 9 (G)
⑰ H. ZONE 9 (R)
⑯ H. ZONE 9 (B)

IC535 ⑱ V. ZONE 2 (G)
⑰ V. ZONE 2 (R)
⑯ V. ZONE 2 (B)

IC536 ⑱ V. ZONE 3 (G)
⑰ V. ZONE 3 (R)
⑯ V. ZONE 3 (B)

IC537 ⑱ V. ZONE 4 (G)
⑰ V. ZONE 4 (R)
⑯ V. ZONE 4 (B)

IC538 ⑱ V. ZONE 5 (G)
⑰ V. ZONE 5 (R)
⑯ V. ZONE 5 (B)

IC539 ⑱ V. ZONE 6 (G)
⑰ V. ZONE 6 (R)
⑯ V. ZONE 6 (B)

IC540 ⑱ V. ZONE 7 (G)
⑰ V. ZONE 7 (R)
⑯ V. ZONE 7 (B)

IC541 ⑲ ————
⑱ V. ZONE 8 (G)
⑰ V. ZONE 8 (R)
⑯ V. ZONE 8 (B)

IC542 ⑲ ————
⑱ V. ZONE 9 (G)
⑰ V. ZONE 9 (R)
⑯ V. ZONE 9 (B)

IC543 ⑲ SHARPNESS
⑱ COLOR
⑰ HUE
⑯ VOLUME

IC544 ⑲ DRIVE (G)
⑱ DRIVE (R)
⑰ DRIVE (B)
⑯ CONTRAST

IC545 ⑲ BACK GROUND (G)
⑱ BACK GROUND (R)
⑰ BACK GROUND (B)
⑯ BRIGHT

IC546 ⑲ BLANKING (T)
⑱ BLANKING (B)
⑰ BLANKING (L)
⑯ BLANKING (R)

3-5. Circuit Board DC

The Dc board consists of : (1) V. OUT circuitry, and (2) SUB. OUT circuitry. Both circuits are common for R, G, and B.

1. V. OUT CIRCUITRY

1) V. OUT···consists of uPC4558 and uPC1498. As it is common to all 3 channels, here the G−ch will be explained. V. OUT waveform is input into pin ③ of connector DC−2 from the DB board.(Fig. 1 A). Although this is input into pin ③ of IC5, since pin ② of IC5 is a GND, a waveform similar to the one shown in Fig. 1 B is feed back and pin ③ of IC5 becomes a GND. Any voltage error that exists between pins ② and ③ of IC5 will be output from pin ① of IC5 (Fig. 1 C) and is received by pin ④ of IC6. The output is through pin ② and a electric current like the one shown in Fig. 2 B flows. As a result a voltage waveform similar to Fig. 1 D is generated. Fig. 1 E is the pulse power supply, and is created by uPC1498 which detects the erroneous portion of the pulse of the input waveform (C) and by accumulating D5 and C10.

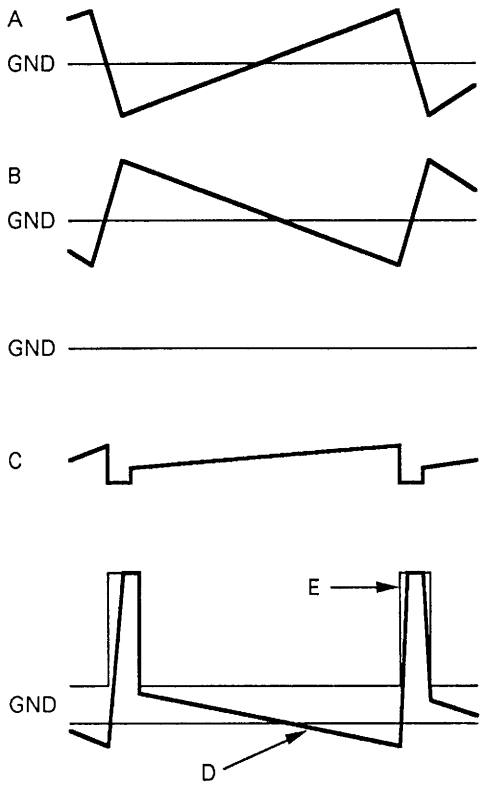


Fig. 1

2) V. STOP PROT.···Slice the pulse at the output (pin ② of IC6) V. OUT. If C14 does not exist, the waveform of collector Q2 will be a pulse waveform such as in Fig. 2 A, practically−speaking, it will be integrated by C14 and become a saw wave like the one in Fig. 2 B. If an abnormality is encountered in V. deflection, as shown in Fig. 1 D, the pulse voltage will disappear and the Q2 collector will attach to +B. When this happens, C14 gradually gets charged as shown by the dotted points in Fig. 2 B and exceeds the pin ⑥ IC5 which is the comparing voltage, causing pin ⑦ of IC5 to become High, Q4 to turn ON, and Q5 to turn OFF. This is the V. STOP mode.

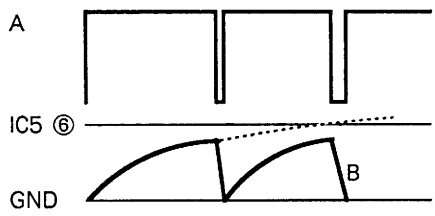


Fig. 2

3) V. PULSE···To output V. PULSE for V. BLK use, slice the V. OUT pulse with IC9 and feed it through D10 and Q6. Note that V. STOP signal is added at D9 so that a BLK is applied during V. STOP.

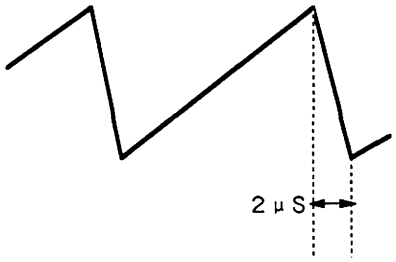
2. SUB OUT CIRCUITRY

1) SUB OUT···Since all of the 6 channels (R, G, B, H.SUB, V, SUB) uses the same circuit, we will explain about H. SUB (R) in this section. The waveform input int pin ① of connector DC−3 will be amplitude−adjusted by IC101. C301 is a reverse adjustment circuit provided as protection against current overloads. Pin ② of IC301 is the input while pin ③ is the return. Pin ⑥ is the out for the voltage error between input and output. As frequency performance is important, the gain for operational amplifire will be kept low and a discrete AMP used. For the discrete AMP section also, we have used an active load rather than a negative load. This constant−current circuit is comprised of D302, Q301, and R318, and has a current flow of 18mA.

2) PULSE POWER SOURCE···The current required to produce a correcting waveform with a retrace of 2 μs and H. SAW waveform with 1.5Ap-p will be -30V, as the following shows :

$$V = -L\frac{di}{dt} = -40\ (\mu H)\frac{1.5\ (A)}{2\ (\mu S)} = -30V$$

For this reason, PULSE power supply is used only for return lines.
AD. HD is added to pin ① of connector DC-13, and the + side PULSE created at Q105 and the - side PULSE at Q108. The PULSE power supply is produced by adding ±15V to each of these PULSES.



3) CURRENT LIMITER···This is a limiter circuit for negative overloads on ±15V lines. The +15V side is made up of Q9, R64, and 76. When current flows through the base-emitter resistance and exceeds the transistor's V_{BE}, Q9 is turned ON and is added to V. STOP PROT. The limiter current is approximately 4A.
Same for the -15V side.

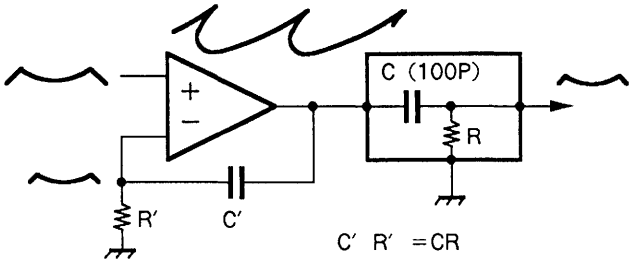
3-6. Circuit Board K

1. DYNAMIC FOCUS CIRCUIT

1) H Dynamic Focus
H parabola waveform input into Pin ⑦ of Connector K-1 is phased-reversed at 1/2 of IC201 (uPC184C) and further amplified by a non-reversible AMP consisting of drivers Q201 and Q202. This is then input into a DFT (Dynamic Focus Transformer). DFT is also capable of providing an amplitude of 300Vp-p at the DFT OUT when the phase is shifted and amplified and when the input is 3Vp-p.

2) V Dynamic Focus
The dynamic focus waveform is added within the focus pack to the focus voltage through condenser integration. Due to pressure and size considerations, a large size condenser could not be selected and the one that was used at this time has a very small capacity of 100PF. Unlike the H waveform, the V waveform has a very low frequency which makes it difficult for the waveform to path, causing a reduction in amplitude and shifting of the phase. In view of this, a circuit like the one shown below was used, enabling us to realize the transmission of the dynamic focus waveform. By placing a time constant that is the same as the time constant in the focus pack within the negative feedback system, it will be possible to send the desired waveform as output.

〈Equivalent circuit〉



2/2 of IC201 (uPC814C) is the operational amplifire of the negative feedback system, Q203 the reversing amplifire and Q204 the output buffer. The time constant of C210 (0.1MF) and R212 (10K) is aligned with the time constant within the focus pack. In practice, since this C, R (C210, R212) is a differentiator, it is not possible to apply the negative feedback system to the direct current portion. For this reason, the direct current portion is first integrated by R214 and C209, and then feed back to R213. The V content requires an amplitude of about 100Vp-p within the focus pack. The output of Q204 has an amplitude ranging from 150V to 400Vp-p and its magnitude is determined by the frequency of vertical. By entering the vertical content, output from Q204 to the secondary side of DFT, the horizontal content is modulated and the total output is input into the focus pack.

2. AUDIO AMPLIFIER

The audio signal input from pin ① of connector K-3 goes through buffer Q205 and is received by IC203 (uPC1241H) which is the amplifire IC. Speakers are driven directly by this IC. Q206 is a series regulator transistor and is used to suppress the power supply's ripples from appearing in the sound.

3-7. Circuit Board Y

1. Power Supply Block (PS1, PS2, D1, D2)

PS1 and PS2 serve as a power cutting fuse when a voltage overload occurs within board Y. In addition, D1 and D2 convert the voltage from +5.7V (−5.7V) to +5.0V (−5.0V). When pressing the main power switch of the set, SUB +5V is supplied, and when pressing the power switch of the commander, ±5.7V is supplied.

2. CPU Block

2−1. CPU (IC1)

A Z80 series 8−bit CPU with SIO, TIMER and other supporting ICs integrated into a single chip is used.

2−2. MEMORY (IC2, 3, 4)

This is made up of programmable ROM (IC2), a general purpose S−RAM (IC3) for flag and data READ/WRITEs, and a non−volatile ROM (IC4) used to record adjustment data, etc.

2−3. BUS BUFFER (IC7, 8)

A hysterisis−type current buffer is used for data transfers to systems external to the Y board (DB and L boards).

2−4. RS422 (IC24)

An RS422 transmitter/receiver for communications with external computers, automatic adjustment devices, etc.

2−5. RESET CIRCUIT (IC5, Q1, 2)

A power−on reset circuit for the CPU and SIRCS DECODE IC. Q1 and Q2 operate so that a normal reset occurs during instantaneous drop in power voltage caused by sudden black out, etc.

3. SIRCS Block

3−1. SIRCS DECODER (IC9), WAIT CONTROL (IC6)

This IC decodes SIRCS signals to enable the codes to be read by the CPU. The following processes take place from the time the SIRCS signals are received until the codes are read by the CPU :

* The "CONT" terminal is set to Low when a valid SIRCS code is received.
* A CPU interrupt occurs and the CPU turns the "CE/OE" signal of IC9 to Low.
* IC6 (mono−multi) puts the CPU in WAIT state for a few msec.
* Finally, the data are read into the CPU.

3−2. POWER CONTROL (Q3, 4, 5)

When IC9 decodes a POWER ON (OFF) code, it unconditionally turns Q3 ON (OFF) and sends (cuts) the current supplied to the "power cont" line, thereby enabling control of the power supply. When the protector is activated, the power supply is cut by externally dropping the "power cont" line to GND. However, it should be noted that in such cases the operation of the protector is detected by Q4 and IC9 is reset by Q5.

4. I/O Port Block

4−1. ADDRESS DECODER, PARALLEL I/O PORT, INTERRUPT CONTROL (IC10, 28)

IC10 is a dedicated gate array with the above functions and is a PORT that is used to READ ch −select and other control/input signal information. Additionally, it receives the control line for each protector and is also equipped with such functions as generating a CPU interrupt while it is in operation.

4−2. DIP SW (SW1, 2)

SW1 is a special switch used for mode adjustments at the factory ; normally all bits (SW1−1 to 4) must be set to ON.

When SW2 is pressed, all adjustment data defaults to the factory setting.

5. fH/fV DETECT Block (IC12)

The present deflection frequency is detected from the VD/HFHD signals supplied by the deflection system and the information is sent to the CPU.

6. SYNC Block

6−1. SYNC CONTROL & CLAMP PULSE GENERATOR (IC11)

This is a gate array that generates SYNC pulses for the deflection system and clamp pulses for the signal system. It uses SYNC signals received from the signal board (H/C−sync, V−sync, Sync on Green) for its input. Itfeatures : * Detection of input SYNC signals (existence or non−existence of each SYNC and its polarity)

* Selection of SYNC source (H/V−sync, Sync on Green or Composite−sync)
* Alignment of SYNC polarity (Reversed when H/V−sync has a positive polarity)
* H/V separation for Composite−sync and Sync on Green
* Phase control of clamp pulses
* Width control of clamp pulses
* Transmission of various function control signals and information through the CPU BUS

6-2. H-SYNC REFORM (IC6)
Maintains the width of H-sync sent to the deflection system for approximately 2 μsec.

6-3. V-SYNC DETECT (IC26)
Detects whether V-sync out pulse of IC11 exists or not and sends this information to the CPU. For example, this is done to determine if the signal connected to H/C-SYNC input terminal is composite or not.

7. CHARACTER GENERATOR/INTERNAL SIGNAL GENERATOR Block

7-1. CHARACTER GEN. INT-SG (IC13, 14, 15, 16, 17)
Whenever an input exists, a clock synchronized to "HFHD" and "VD" are used to generate each test pattern and character. When input does not exist, the H and V-sync pulses, test patterns, and characters are created by a crystal-oscillated clock. (IC13)
IC14 is a high-speed S-RAM to record the position and color of the screen characters, while IC15 to 17 are mask ROMs to record character font data.

7-2. TTL to ECL CONVERTER (IC18, 19)
Because INT SG, character R/G/B, and BOARDER (shadow of characters) signals contain high-frequency contents, they are converted to ECL before being sent to the signal system board.

7-3. PLL (IC20, 21, 22, 23, 25, Q6)
Characters and internal signals are generated by synchronizing them with the incoming signals (HFHD and VD to be precise) with the use of a PLL circuit. The output from the phase comparator system (IC20) passes through an active filter composed of C44, R94, 95, and IC20 are then fed into a VCO (IC21). The output from VCO first goes into IC13 "CKIN" and then passes through a 1/417 pre-scaler equipped within IC13. Finally, the output is returned to the phase comparator.
Since a single VCO imposes a limit on the frequency range that can be locked, 2 VCO units (IC21 is actually composed of 2 VCO units) are used : one for high-band use and the other for low-band use. The VCOs are switched by IC22's voltage converter and the flip-flop of IC23.
Furthermore, to improve the stability during locked conditions, Q6 and IC25 are used to control the polarity of the correcting waveform of IC20 pin ③.

7-4. VD SYNCHRONIZE (IC26, 27)
When VD and HFHD are in a certain phase relation, IC13's internal counter deviates by 1 count and may cause V-jitter of the characters. For this reason, the phase of VD is shifted to a stable position.

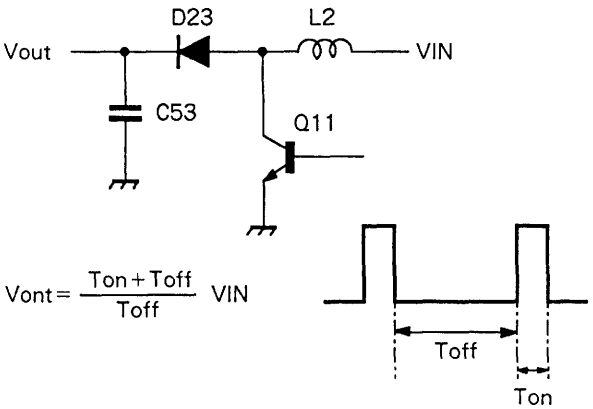
3-8. Circuit Boards PA and PB

1. HIGH-VOLTAGE GENERATOR

As this is a wide-range multiscan compatible unit, it is difficult to construct a high-voltage circuit by synchronizing with fH as in previous circuits. Therefore, an asynchronous type high-voltage generator having its own oscillator was devised.
The oscillating element X1 is the oscillator's basic clock and oscillates at approximately 500KHz. This clock is divided by IC7 and IC8, generating a 15.625KHz pulse as its internal oscillator (INT OSC). This pulse is output from pin ⑤ of IC8 and this INT OSC is used as a switching pulse between two circuits, one of which is sent through buffer Q3 and used in the high-voltage generator circuit. The other passes through buffer Q4 and connector PA-3 and becomes the switching pulse for the negative power supply for board E. The pulse passes through buffer Q3 and connector PA-7 and added to Q6, the transistor used to drive transformer Q6. The output of this drive transformer (T2) drives FBT's converter Tr (Q10). Q19 is the power current source for controlling the drive condition of converter Tr (Q10). By fixing its base and by adding the same voltage as +B of FBT to the emitter resister (R112), it modifies the energy of the primary side of the drive transformer in accordance with the HV load, enabling converter Tr (Q10) to be driven most efficiently. The basic section of the high-voltage circuit is the same as with previous circuits in which Q10 is the converter Tr ; D20 and D21, the damper diode ; C51, the common condenser ; L3 and L4, the dummy L ; and C54, an S-shaped condenser. To realize high output to FBTs are connected in parallel. From one of them (FBT 1) the MV for use as the focus voltage is extracted.
As this particular system uses an asynchronous high-voltage method, the high voltage's ripple content can easily affect the screen. For this reason, the high voltage generated by FBT is once passed through a filter (HVF) and then is added to HVB which distributes and detects high voltage. This is then supplied to each CRT.

2. HV REGULATOR

In a high-voltage regulation method, +B of FBT is controlled (FB pulse level controller) to maintain a constant high-voltage level. The +B that is being controlled is made by stepping up a +100V by a switching regulator circuit. The degree of step up is determined by the duration of switching ON and OFF. When the ON duration is long, the degree of step up is greater and vice versa. The high voltage is reduced by a factor of approximately 4125 by HVB and the output passes through connector PA-7 and goes into buffer IC1 (uPC4082, 1/2). This buffer output is further divided by high-voltage adjustment resistors △R41 and △R42 and is input into the plus side (pin ①) of operational amplifire switching regulator IC6 (uPC1394). The minus side (pin ⑭) is supplied with the voltage (approximately 3.0V) of IC9, the standard voltage source. It is through this difference in voltage that the ON-OFF Duty of switching pulse (pin ⑦ output) is modified. The output of pin ⑦ passes through buffer Q20 and into the drive converter circuit Q5 and T1. There, the polarity of the pulses are reversed and the switching transistor Q11 driven. Q11 steps up the +100V voltage by switching L2 and regulating with D23 and C53. If the high voltage rises and exceeds the voltage (pin ① of IC6) of the detector side, the ON interval of Q11 shortens and +B is lowered, causing the high voltage to fall. In case the high voltage level falls, a completely opposite operation takes place. As this goes to show, a negative feedback is applied so that the high-voltage detector voltage is always equal to the standard voltage (approx 3.0V).



3. HIGH VOLTAGE PROTECTOR

1) HV Protector

This is a protector to suppress any abnormal rise in HV due to some accident. The HV voltage is divided by the high voltage block (HVB) and by △R33, △R34 and is input into the plus side of 1/2 of IC2 (uPC393C). A comparator voltage (approximately 4.8V) generated by zener (RD5.1ESB2) should be input into the minus side. The protector is activated when HV rises and the voltage on the plus side exceeds that of the minus side. It operates by first turning the 1/2 side of IC2 (uPC393C) ON and the 2/2 side OFF. The oscillation of the HV Regulator is stopped by D8 (ISS119) and Q7 is then turned ON. This causes the oscillation of the converter to be stopped. After dropping HV, D28, Q16 and Q15 are turned ON and the power turned OFF.

2) Σ IK Protector

This protector suppresses any abnormal beam to flow through the CRT. The current of FBT's secondary side is changed to a voltage by R44 to R47, R119, R120 and the protector is activated when this voltage exceeds a certain level. This detecting voltage is divided by R121 and R1 and is input into the base of Q1, which is usually set to the ON position. As the beam current gets larger, the detecting voltage lowers rapidly to the minus side until it reaches a point where Q1 is turned OFF and the protector is activated. The method of operation is the same as (1) HV Protector. The oscillation of the regulator is first stopped, the HV dropped, and finally the unit's power turned off. The unit consists of 2 channels of identical Σ IK protectors.

3) Low B Protector

This protector is activated when IC5 (uPC78M12H), an IC that generates Low B (+12V) inside board PA, is destroyed and as a result Low B (+12V) increases. A voltage generated by resistance dividing Low B (+12V) is input into the plus side of IC1 (uPC4082C) 1/2 while a comparator voltage generated by zener (RD5.1ESB2) should be input into the minus side. The protector is activated when Low B rises and the voltage on the plus side increases.

4) Regulator Protector

This protector protects the element by turning off theoscillation of the regulator when the regulator's voltage becomes abnormally high such as when a high voltage load has been opened. The voltage at the regulator out is divided by R48 to R50, R14, R15 and is input into the plus side of IC3 (uPC393C) 1/2. A comparator voltage should be input into the minus side. When the voltage at regulator out rises, this operational amplifire is enabled and the protector activated.

VPH-1270Q
RM-1270

4. INTERNAL PROTECTOR

The circuit is designed so that when certain abnormal modes (for example, when deflection is disabled) are encountered the power is immediately cut off to avoid secondary disasters within the unit. Among the devices, H STOP (horizontal deflection disabled), V STOP (vertical deflection disabled), and FAN PROT (fan protector) all have their power-cut unit centralized on board PA. H STOP and V STOP send their output to the respective open collector and an OR operation is performed with B24 and D25. During abnormal conditions, Q16, Q15 turn ON and brings the "POWER CONT" line to low, thereby cutting off the power. Since the polarity of the "FAN PROT" signal is the opposite of H STOP and V STOP with normal ON generating output, the signal is reversed by Q17 and input into Q15.

3-9. Series E Board Circuit Operation

1. F-V Conversion

H-KEY, H-PIN and H-SIZE are input throught E-1 connector and added at IC106 (1/2). This output,

(a) passes R131 and is input to IC105.

(b) is input to IC106 (2/2) and compared with H-SIZE detection output. The error difference is input to IC103 (2/2) and fully integrated and amplified, which then passes R186 and is input to IC105.

It is again fully integrated at IC105 (1/2). This DC passes R103 and switched by Q101. IC101 (1/2) generates pulse which is synchronous to 5 μs width fH and inputs it to Q101 gate.

Here, voltage proportional to H-SIZE voltage and fH, is generated. This output passes IC102 buff, is integrated at R111, C105, R109 and C104, and output at IC104 (1/2) to complete F-V conversion.

2. Negative Power Section

F-V conversion output and negative power is compared at IC104 (2/2) and added to IC111 pin ①.

IC105 (2/2) generates bias and adds it to IC104 (2/2). IC111 is a switching regulator. IC, and outputs pulse which complies to pin ⑭ and pin ① voltage, to pin ⑦. This pulse is switched at Q109 and drives Q107, 108, and the output drives Q110 through T105.

Pulse output to Q110 source is rectifide at D112, C124 to generate negative power. R208 is for current detection and IC111 pin ⑤ is connected at top end to protect against over current.

3. PIN MOD Section

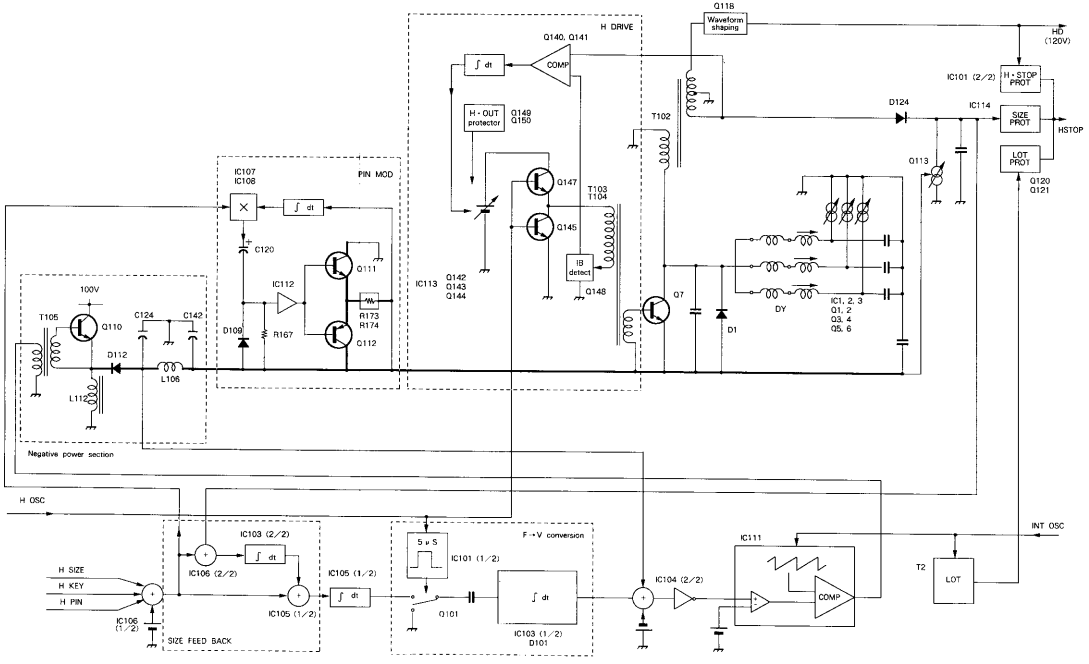
H-KEY, H-PIN correction wave is input through E-1 connector, added at IC106 (1/2) and output from pin ⑦. This output passes IC110 and is input to IC107 pin ④. On the other hand, PIN MOD OUT voltage divided by R150, R285 and R149 is input to IC107 pin ⑨. With these two inputs, PIN MOD correction voltage which corresponds to fH H-SIZE is output to IC107 pin ⑭. This output is amplified at IC108, passes Q103 and Q104 buff, and is input to IC112. When this occurs, PIN MOD correction wave is clamped to negative power by IC109. IC112 operates around negative power electric potential. Q111, 112 are driven by voltage output from IC112 pin ①and PIN MOD OUT voltage is output to Q111, 112 source.

4. H-DRIVE Section

H, OSC is input from E-1 connector pin ⑤, passes R233 and input to Q130, 131 base. The signal is divided into two by Q130, 131 emitter.

One signal passes C161 and input to Q145 gate. Q145, 146, 147 are transistor for per-drive. These transistor switch Q7 (H,OUT) through T103, 104 (HDT). The other signal passes R234 and is input to IC113 (1/2). IC113 output pulse becomes saw-tooth wave at R238, C150. Q132 is a constant current source. Pulse is compared at Q133 and 134 to control Q132 constant current source and keep saw-tooth wave amplitude constant.

This saw-tooth wave and IB2 constant circuit output voltage, which will be explained later, are compared at IC113 (2/2) and the pulse difference is output to IC113 pin ⑦. This pulse passes Q135, 136 buff and input to Q142 gate. Q142, D118 and C159 construct a STEP UP regulator. Normally, 100V is supplied to Q143 and Q144 collector, but when Q142 switch, the additional voltage is supplied to Q143 and Q144 collector, Q144 emitter is connected to Q146, 147 collector. Normally, 100V power is supplied through Q143, 144 series regulator, but when more drive is needed, Q142 operates to supply power over 100V.



(IB2 Constant Circuit)

Current (IB) which flows on the primary side of T103, 104 (H. D. T) is detected at R267, 268 and generated as voltage at Q148 collector. This voltage passes R225 and input to Q140 base. In the meantime, H. O. T. secondary side H. Pulse divided by R259, 260 and R259 is input to Q141 base. By comparing the peak voltage of the two, IB2 is always remaind constant.

H. Pulse > At IB2 peak (under-drive)

Q140 cut off→Q139 base potential rise→Q139 collector potential lowers→Q137 base potential lowers→Q137 collector potential rises→Q144 emitter potential rises→ to over-drive.

H. Pulse < At IB2 peak (over-drive)

Q141 cut off→Q139 base potential lowers→Q139 collector potential rises→Q137 base potential rises→137 collector potential lowers→Q144 emitter potential lowers→to under-drive.

Feed Back is conducted as above.

5. H-SIZE Feed Back Section

H. O. T. secondary side H. Pulse is peak rectified at D124 to convert it to H. SIZE detection output.

Q113 is a variable current source, and works to get the same detection out puteven when fH is different at the same pulse height. This output is returned to IC106 (2/2), compared with input and the error difference is controlled.

6. HD Output Section and H. STOP Protector Section

AFC HD clamps H. O. T. secondary side H. Pulse at C144, D113, re-shapes the wave at Q118, passes pulse through Q116, 117 and outputs from E-1 connector pin ⑨.

HD output from Q116, 117 emitter is input to IC101 pin ⑪. As long as HD is input to IC101 pin ⑪, pin ⑩ is High. Therefore, Q115 is ON and H. STOP line is normally Low. If HD is not input, IC101 pin ⑩ becomes Low and Q115 turns OFF and as a result, H. STOP line becomes High and set power turns OFF.

Other protectors are H-SIZE MAX/MIN protector and 100V line LOT circuit over current protector.

IC114 detects H-SIZE MAX/MIN.

When H-SIZE becomes too large, IC114 pin ① becomes Low.

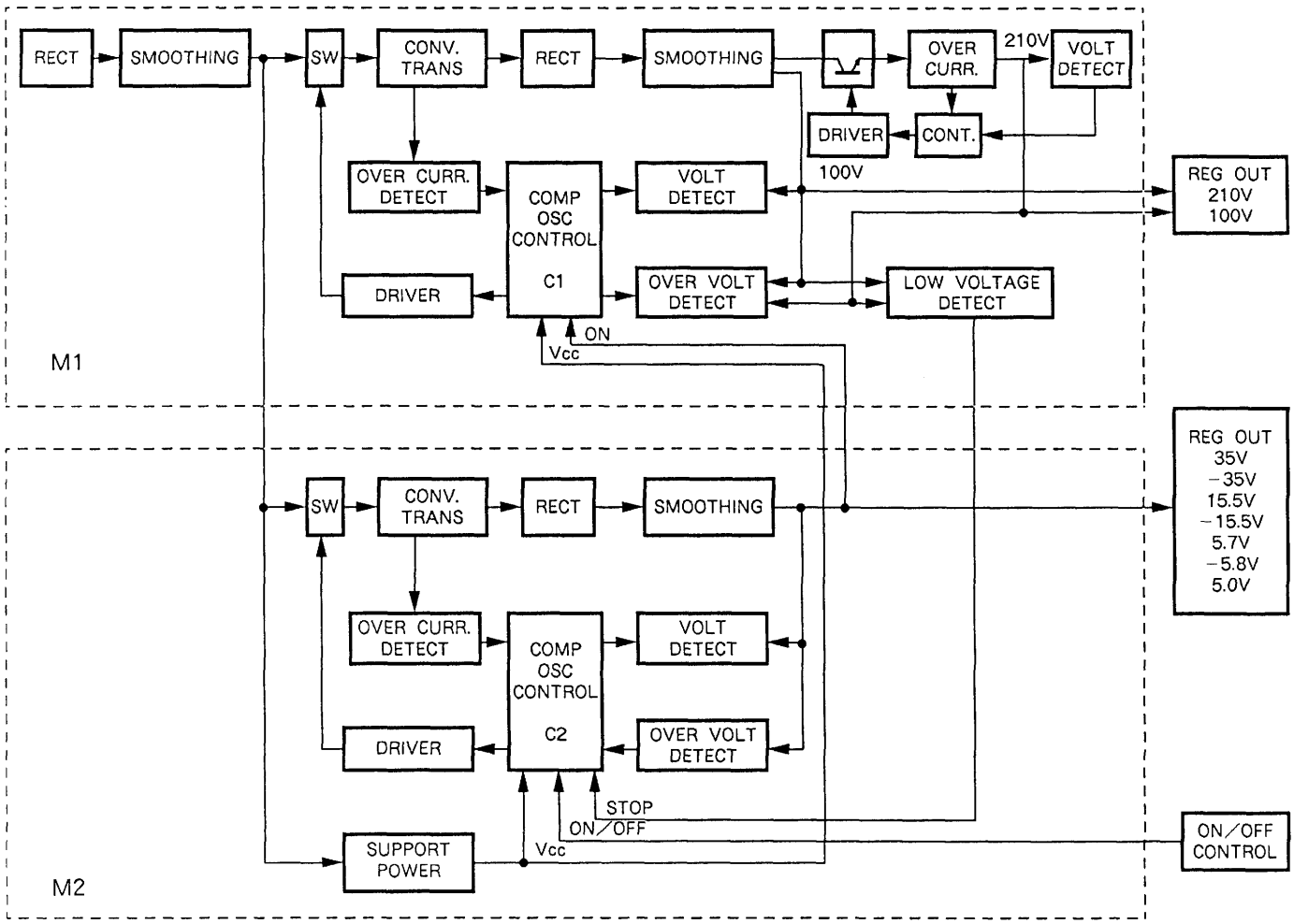
When H-SIZE becomes too small, IC114 pin ⑦ becomes Low.

This output passes D139 and connects to IC101 pin ⑬. When pin ⑬ becomes Low, IC101 pin ⑩ becomes Low and protector actuates.

LOT circuit over current protector detects current at R221. When there is over-current, first Q120 turns ON and then, Q121.

Q121 collector is connected to IC114 pins ①, ⑦ line, and protector actuates as above.

3-10. SOPS-1008



This power source is composed of 2 half bridge converters and 1 self-excited flyback converter (auxiliary power source.) When the main switch is turned ON, at first the auxiliary power source operates, voltage is supplied to boards C1, C2 of the board M1, and their respective control IC (IC51) operate. At this point, the power source doesn't operate, but instead, ON signal (about 5V) is input from outside, and the power source of board M2 starts operating.

As the power source of board M2 operates, outputting a voltage, a part it is supplied to pin ③ of board C1. This becomes the ON signal, causing the power source of M1 to start operating.

3-11. Board C2 (Control Board)

Pins ①, ② of IC51 constitute the error amplifier for controlling the output voltage. The output of 5.7V is divided by R71,270, RV2551 and input to pin ①. As reference voltage, the voltage (+5V) that is supplied from pin ⑭ is divided by R62, R63, and is input to pin ②. Pin ④ is for dead time control, and while it is "High", on duty becomes "0".

Since pin ④ remains "High"while ON signal is "Low" (ON signal is input via Q251, 258), power source doesn't operate. Oscillation frequency is determined by pins ⑤, ⑥. Pins ⑧, ⑨, ⑩, ⑪ make the output transistor terminal of IC51, and main transistor is driven via T153, T154. Pin ⑭ is the reference voltage (5V) output, and pins ⑮, ⑯ make the error amplifier for overcurrent protection. The voltage detected by T152 is smoothened out with rectifier L1, C53, by D61, 62, 63 ; and is then input to pin ⑯.

3-12. Board M2

C152, 153, 166, 167, Q151, 152, T151 constitute the half bridge converter. The AC voltage that is output from T151 is rectified by D251, 252, 253, 254, 255, 256, and then smoothened by L251, 252, 253, C265, 266, 267, 268, 270.

D276, 277, 278, 279, R265, 266, 261, 263, IC252 constitute the overcurrent protection circuit. If any of their respective output voltages exceed the reference voltage, pin ① of IC252 turns "High", pin ⑨ (IC2) is input into, D58 turns ON, Q53 turns ON, pin ④ (IC5) turns "High", and the operation halts.

3-13. Board C1 (Control Board)

Operation of this board is identical to that of board C2.

3-14. Board M1

C109, 110, 111, 112, Q101, 102, 103, T1013 constitute the half bridge converter. The AC voltage that is output from T101 is rectified by D201, 202, 203, 204, 205, 206, and then smoothened by C201, 202, 213, C214, 215, 216.
Q204, 205, R232, 233, Q206, 207, R234, 235, 236 constitute the overcurrent protection circuit.
In case of 10V output, if the voltage that is divided by R232, 233 exceeds +5V, Q204 turns ON, "High"signal is input to pin ⑨ (IC1), D58 turns ON, Q53 turns ON, pin ④ (IC51) turns "High", and the operation halts.
IC203, R247, 248, 249, 250, 251 constitute the low voltage protection circuit.
In case of 100V output, the voltage that is divided by R247, 248 is input to pin ⑧ (IC203), making it the reference pin ⑤. When the voltage of pin ⑥ becomes lesser than that of pin ⑤, "High" is output through pin ⑦, which is then input to pin ③, time is delayed by C227, R241, "High" signal is output through pin ①, which is then conveyed to pin ⑨ of board C2 of the board M2, and the operation halts.
R201, IC201, R217, 218, RV202 constitute the series regulator. And, R208, 209, 210, 212, 213, 214, 215, 254, RV201 constitute the overcurrent protection circuit.